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VOICE OF THE ENGINEER

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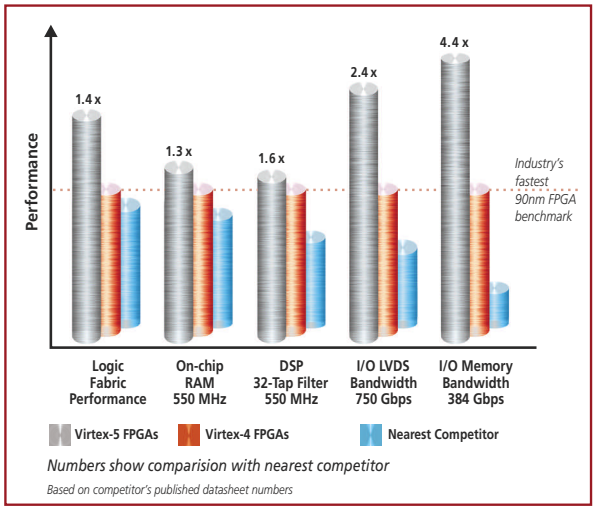

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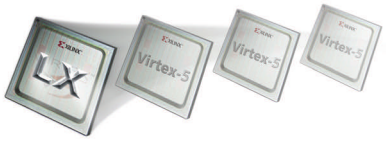

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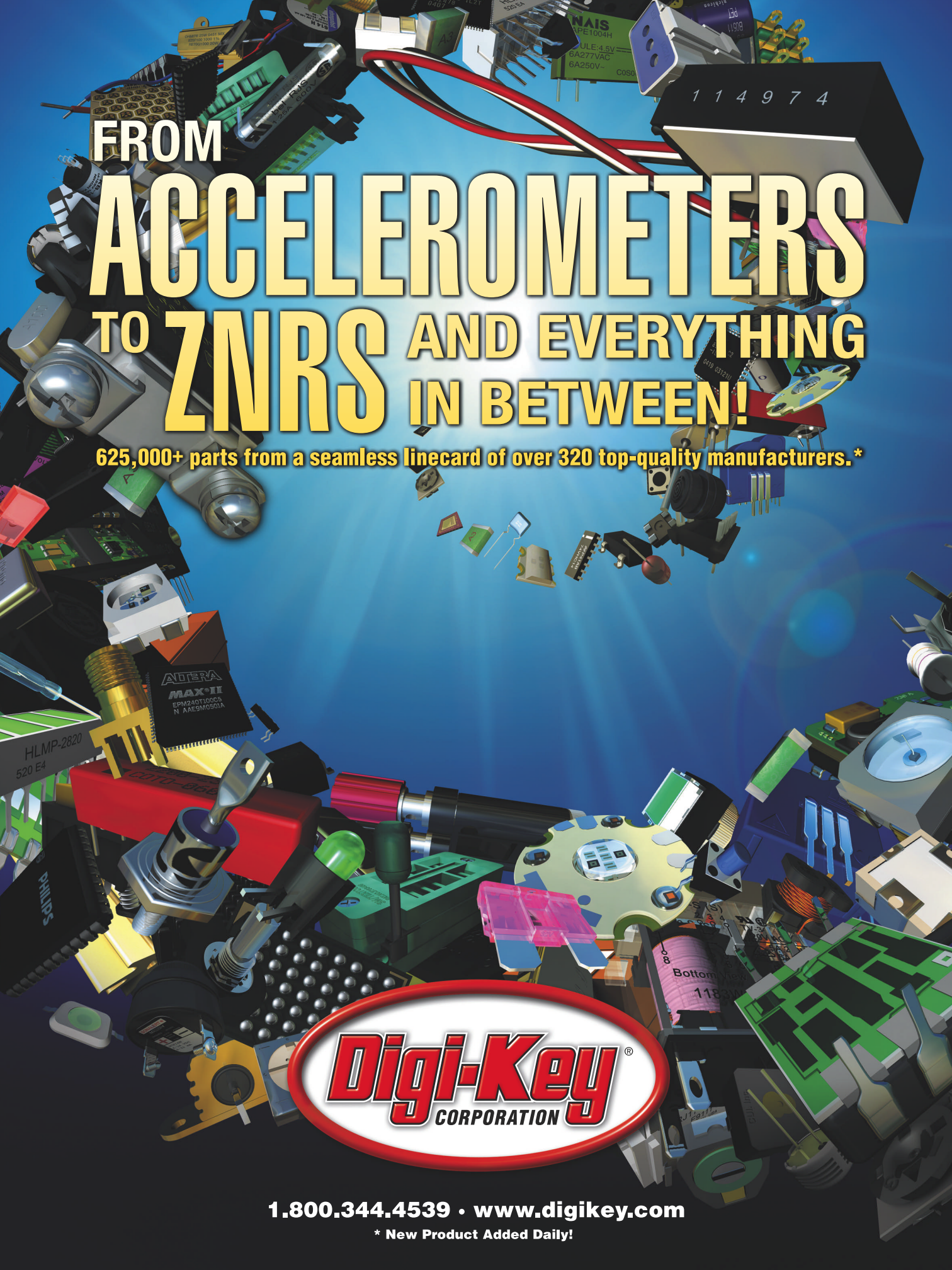
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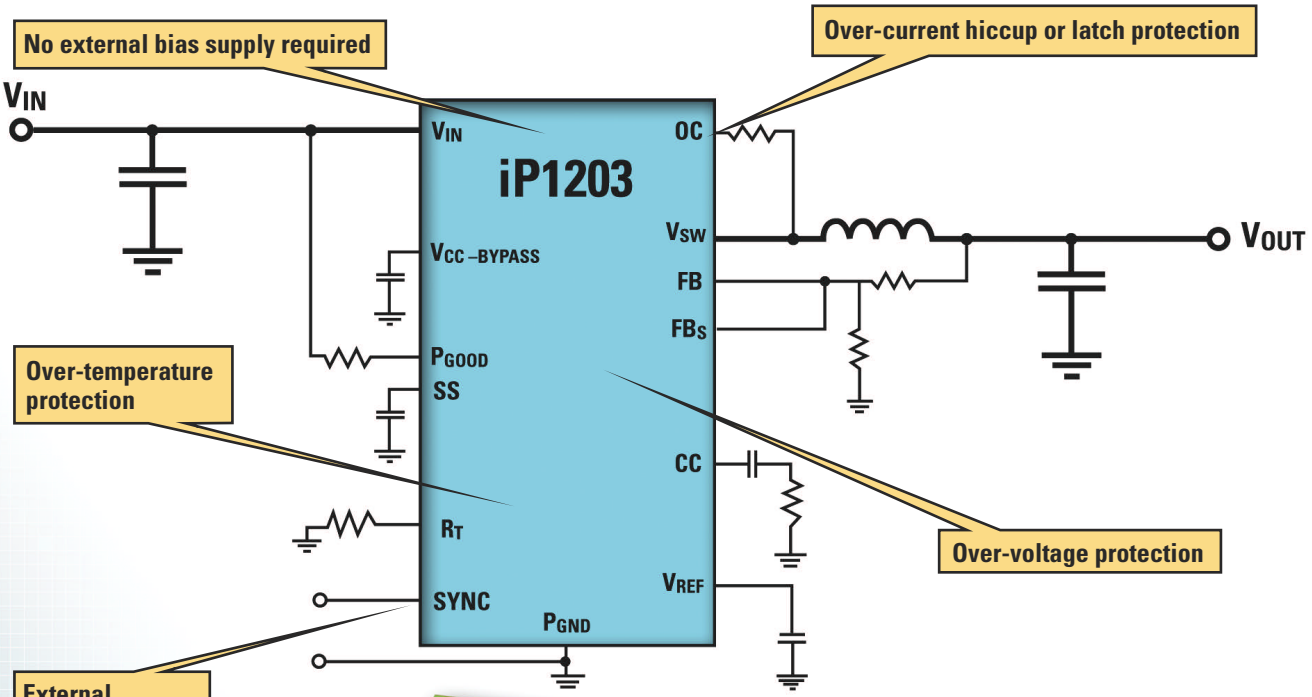
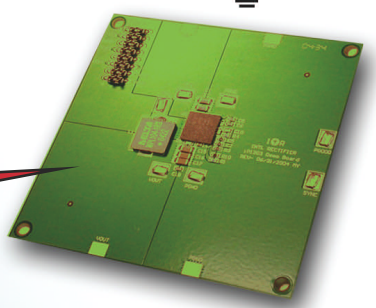


Reference Designs Available

IRDCiP1201-A
IRDCiP1202-A
IRDCiP1203-A



Part #	Package	V_{IN} (min/max)	V_{OUT}	I_{OUT}	Frequency
iP1201	BGA 9.25mm x 15.5mm x 2.6mm	3.14V to 5.5V	0.8V-2.5V for 3.3V_{IN} 0.8V-3.3V for 5V_{IN}	15A dual 30A single	200 - 400kHz
iP1202	BGA 9.25mm x 15.5mm x 2.6mm	5.5V to 13.2V	0.8V-5V for 12V_{IN} 0.8V-3.3V for <6V_{IN}	15A dual 30A single	200 - 400kHz
NEW iP1203	LGA 9mm x 9mm x 2.3mm	5.5V to 13.2V	0.8V-8.0V for 12V_{IN} 0.8V-3.3V for <6V_{IN}	15A single	200 - 400kHz

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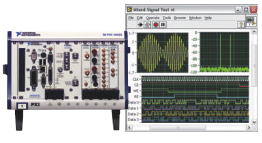

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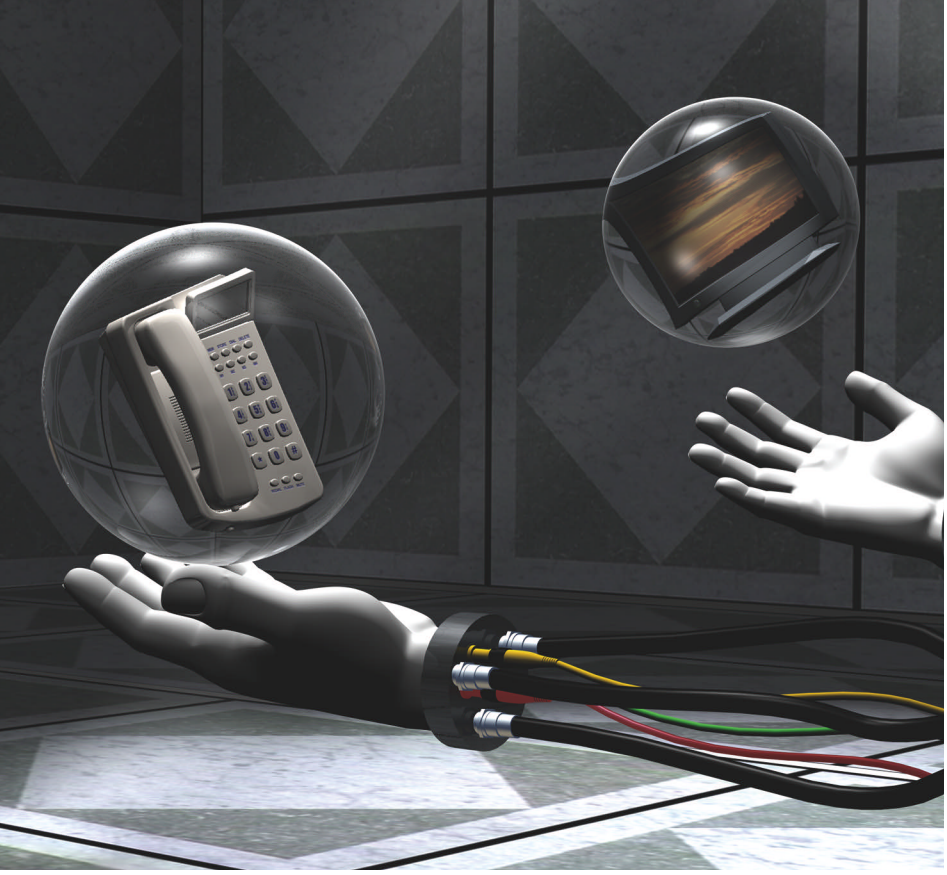

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50 years

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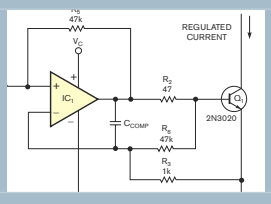

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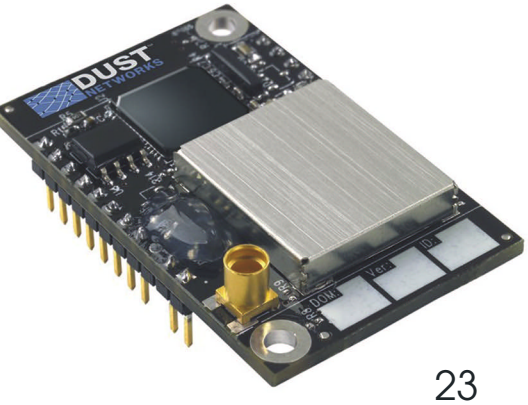

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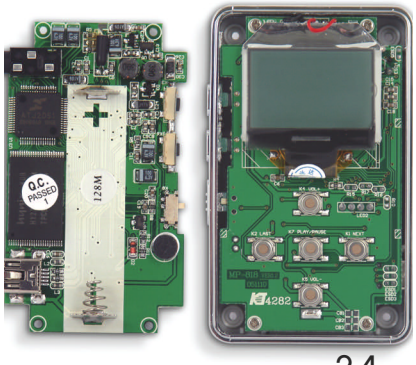

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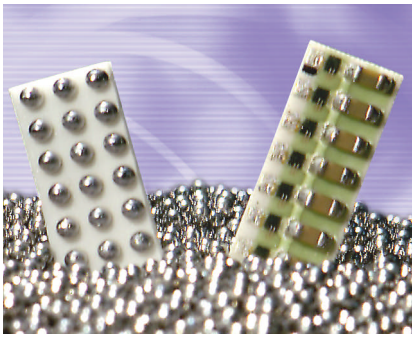

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DEPARTMENTS & COLUMNS

PRODUCT ROUNDUP

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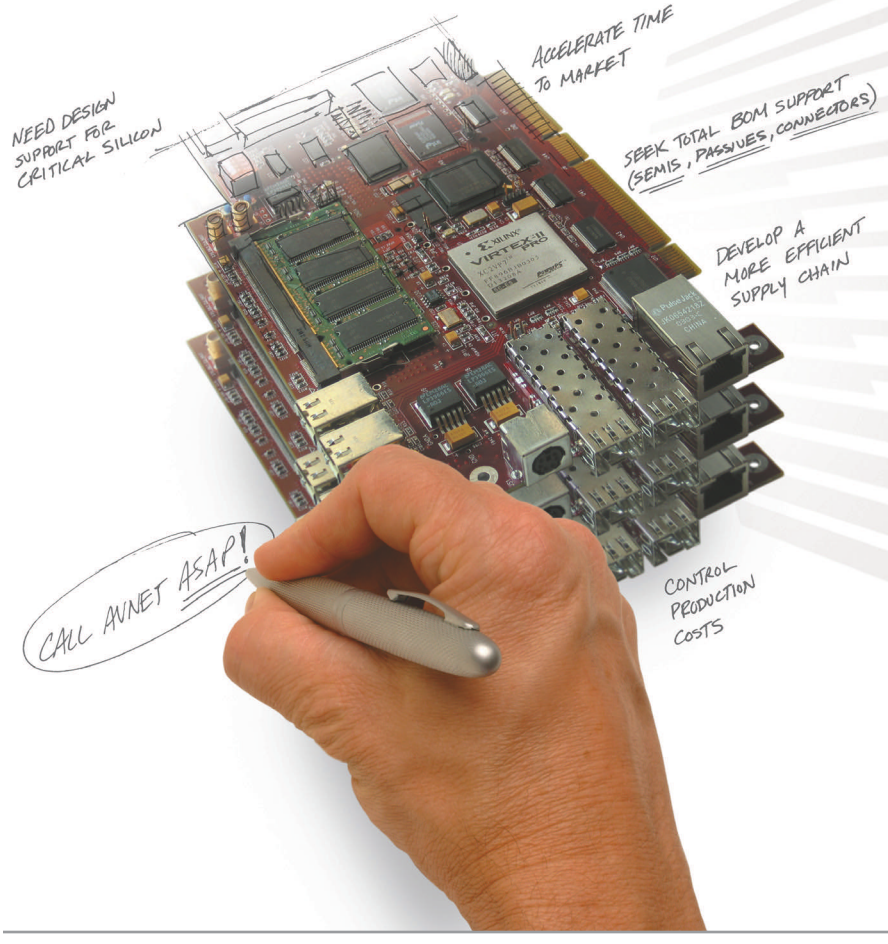

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No. 106

Timing is Everything – The Broadcast Video Signal Path

— By Mark Sauerwald, Applications Engineer

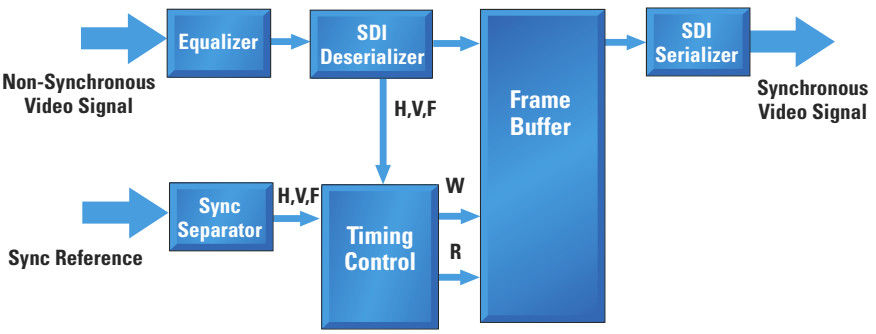

Figure 1. Major Components of a Genlock System

A casual observer would note that there are many different broadcast video studios in the world, operating in different formats, some of them analog and some digital. There are multiple high definition television raster formats in use in the United States today. If you tried to count the number of different raster formats covered by the SMPTE292M HD standard, you would run out of fingers and toes. Within any studio there are many different signals, and they are all synchronized in lock step with one another. In video parlance, they are "genlocked."

Genlocking allows for easy switching from one signal to another (i.e., regular programming to commercials) without disrupting the synchronization circuits that are in the viewer's receiver. To do this requires that any signal coming from an outside source be genlocked to the rest of the signals in the studio. Most studios use an analog signal as their timing reference signal, and the timing information needs to be extracted from this signal to allow it to be used to genlock the incoming signal.

When a new signal is brought into a studio, whether it is coming from a satellite receiver, a camcorder, or any other source, the first thing to do is to synchronize it with the rest of the signals in the studio using a genlock circuit.

Figure 1 shows a block diagram for a genlock which takes an SDI (Serial Digital Interface) input signal, and synchronizes it with an analog reference

NEXT ISSUE:
Delay Calibration

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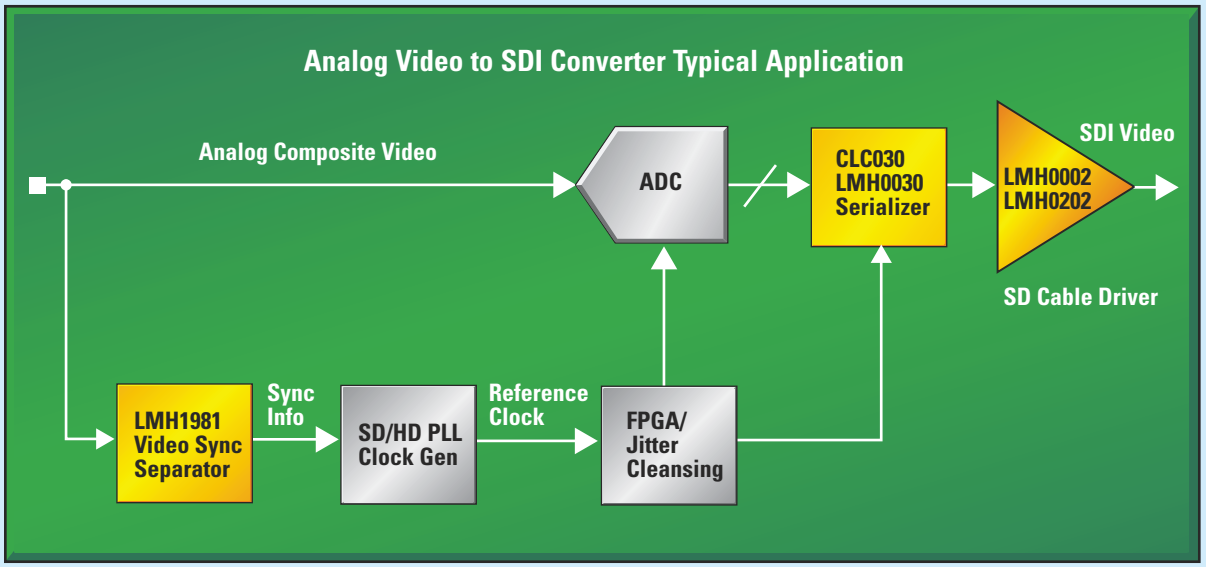
High Performance Analog Video Solutions



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Product ID	Type	Supported Video Formats	Inputs	Outputs	Spec Supply Range (V)	Packaging
Sync Separators						
LMH1981	50% slicing	NTSC, PAL, SECAM, 480i/p, 576i/p, 720p, 1080i/p	0.5 to 2.0 Vpp	H-sync, V-sync, odd/even, burst/clamp, video format, composite sync	3.3 to 5	TSSOP-14
LM1881	70 mV fixed	NTSC, PAL, SECAM	0.5 to 2.0 Vpp	V-sync, odd/even, burst/clamp, composite sync	5 to 12	SOIC-8, DIP-8
Video Converters						
LMH1251	YPbPr to RGBHV converter	480i/p, 576i/p 720p, 1080i, 1080p XGA, SXGA, UXGA	YPbPr	RGBHV	5	TSSOP-24

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Product ID	Type	SSBW (MHz)	A_V (V/V)	Slew Rate (V/µs)	I_{CC} (mA/Ch)	Spec Supply Range (V)	Packaging
Analog Crosspoint Switches							
LMH6582	16 x 8	500	1	3000	110 mA (total)	±3.3V to ±5V	TQFP-64
LMH6583	16 x 8	500	2	3000	110 mA (total)	±3.3V to ±5V	TQFP-64
Analog Multiplexers							
LMH6570	2:1 Mux	500	2	2200	15	6 to 12	SOIC-8
LMH6572	Triple 2:1 Mux	350	2	1400	23	6 to 12	SSOP-16
LMH6574	4:1 Mux	500	2	2200	13	6 to 12	SOIC-14

For more information on National's video amplifiers, visit www.national.com/see/videoamps

that is being supplied. In this edition of the Signal Path Designer, we will look at this application in detail, and examine the design considerations for each of the six blocks.

Cable Equalizer

The SDI inputs on video broadcast equipment typically support long cable lengths: over 140m for high definition signals, and over 300m for standard definition signals. In order to support long cables, there needs to be a cable equalizer.

Long cables have a low-pass characteristic, where the attenuation of the input signal is proportional to the length of the cable, and the square root of the frequency. ***Figure 2*** shows the frequency response of a 100m length of a common (Belden 1694A) cable used in video installations.

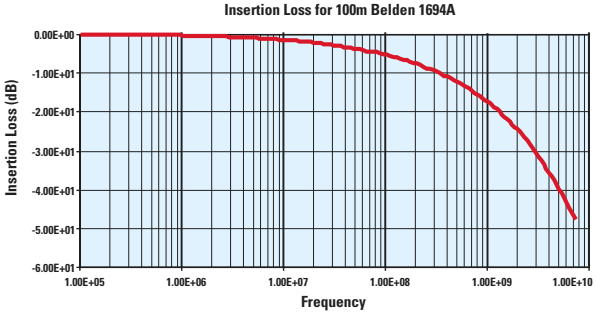


Figure 2. Belden 1694A Frequency Response

Although seeing the attenuation with frequency is helpful in designing the complementary filter that you will need to recover the signal, the image that you really want to see is the eye diagram. This tells you if there is there an opening big enough to recover the data. ***Figure 3*** shows the eye diagrams for a 1.5 Gbps signal (an HD-SDI signal) after it has gone through various different lengths of cable. From the standpoint of this article, the primary result of the skin effect is that as the frequency increases, a smaller and smaller portion of the cross section of the cable will be carrying the signal, so there will be greater signal attenuation at higher frequencies than at lower frequencies. The response curve for this loss will be proportional to the $\sqrt{\omega}$ which makes compensation difficult for standard types of filters.

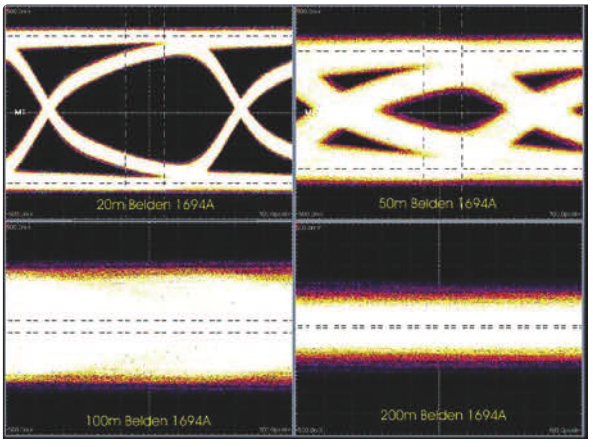


Figure 3. Oscilloscope Traces of an HD-SDI Signal After Going Through Coax Cable

To attempt to match the frequency response of the cable, the designer carefully places the zeroes in his or her filter such that the resulting response is a close approximation to the $\sqrt{\omega}$ response of the cable.

To deal with the fact that both high gain and high bandwidth are required at the same time, equalizer circuits are realized in exotic, high-speed processes such as the National's 0.25 µm BiCMOS SiGe process. An example of one of these equalizers is the LMH0044 cable equalizer. With this part, you can recover signals at data rates of up to 1.5 Gbps through 200m of Belden 1694A cable.

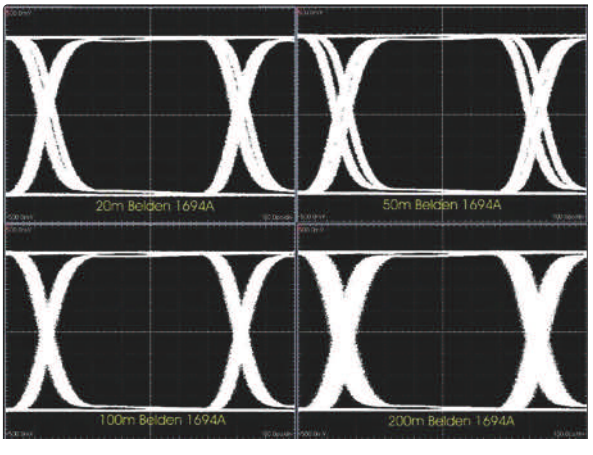
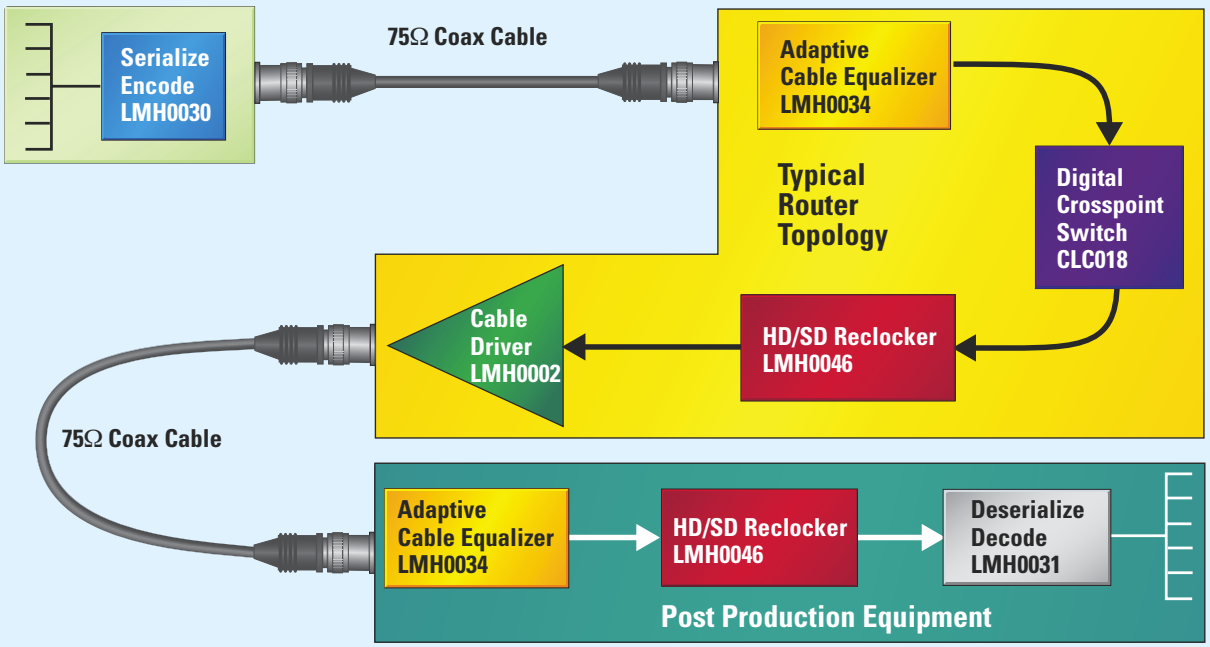
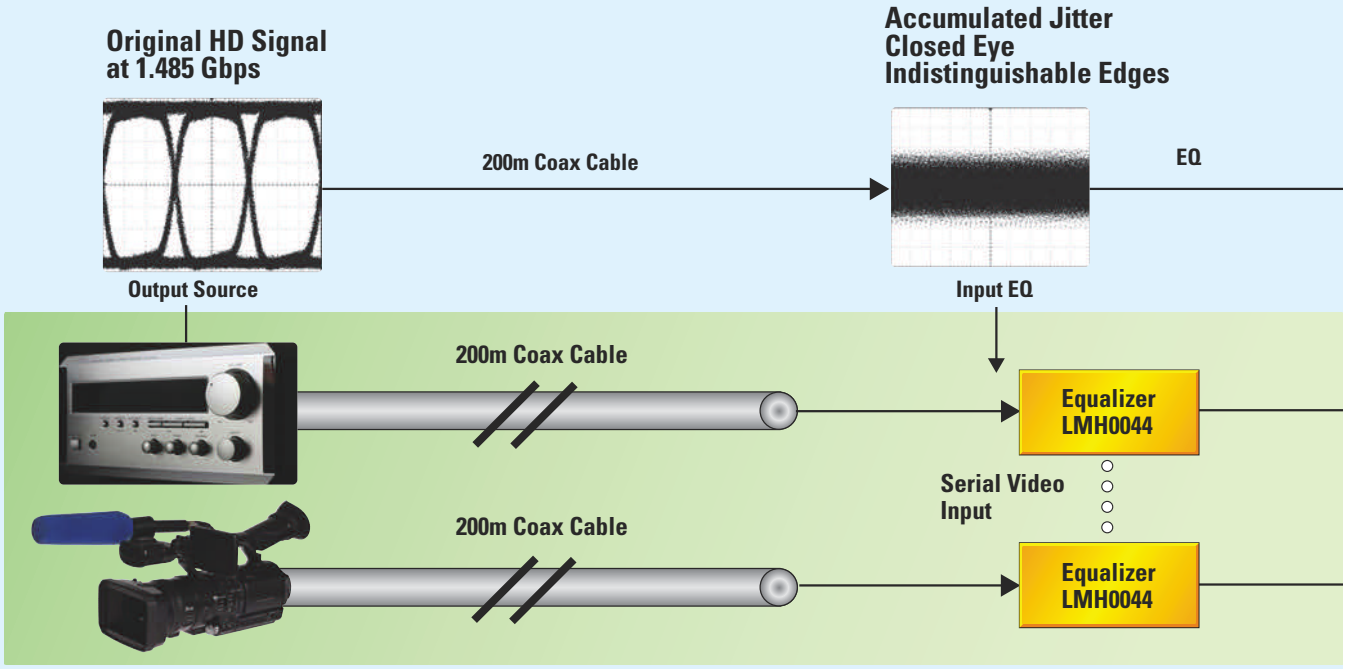


Figure 4. Equalized Outputs

HDI-SDI Signal Path Solutions

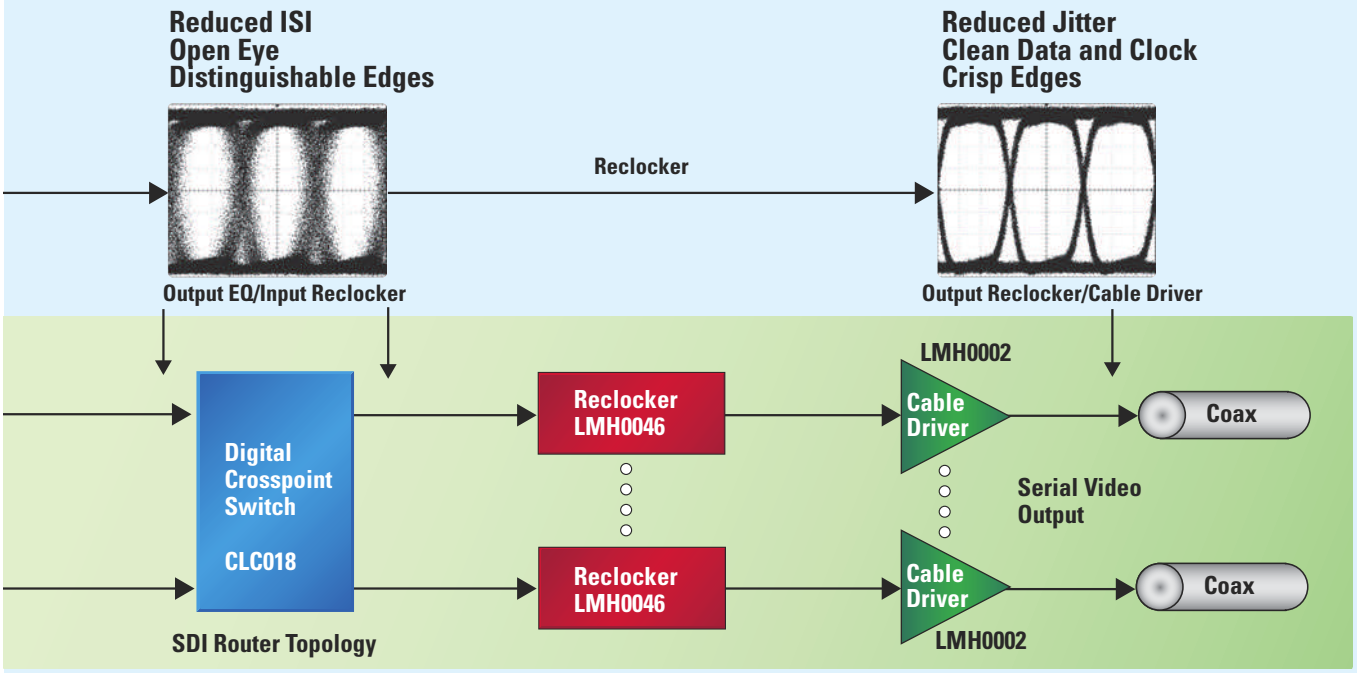


SDI Signal Conditioning



For more information, be sure to visit National's Broadcast Video Owners's Manual at www.national.com/see/bvom

Product ID	Function	Max Speed (Mbps)	Temp Range (°C)	Eval Board	Comments	Packaging
Cable Drivers						
LMH0002MA	HD/SD Serial cable driver	1485	-40 to 85	SD002EVK	Selectable slew rate	SOIC-8
LMH0202MT	Dual HD/SD Serial cable driver	1485	0 to 70	SD0202EVK	Dual differential input, dual differential output	TSSOP-16
Adaptive Equalizers						
LMH0034MA	HD/SD Adaptive cable equalizer	143 to 1485	0 to 85	SD0342EVK	SMPTE 292M/259M Serial recovery	SOIC-16
LMH0024MA	3.3V SD Adaptive cable equalizer	143 to 540	-40 to 85	SD024EVK	Footprint compatible with LMH0034	SOIC-16
LMH0044SQ	HD/SD Adaptive cable equalizer	1.485 Gbps	0 to 85	SD044EVK	Equalize up to 200m of cable at HD (1.485 Gbps)	LLP-16
Encoder/Decoders						
LMH0030VS	SMPTE 292M/259M Digital video serializer/encoder	270 to 1485	0 to 70	SD130EVK	Integrated cable driver, FIFO, BIST, and TPG	TQFP-64
LMH0031VS	SMPTE 292M/259M Digital video serializer/ decoder	270 to 1485	0 to 70	SD131EVK	FIFO, BIST, and TPG	TQFP-64
Reclockers						
LMH0046MH	HD/SD Reclocker	1.485 Gbps	-40 to 85	SD046EVK	Dual differential outputs, optional data rate clock; 27 MHz reference	TSSOP-20



Broadcast Video Signal Path

Deserializer

Once you have done the hard work of opening the eye of the signal coming in, you have to make sense of the bits that are coming at you, and this is the job of the deserializer. Video images have a very regular, repetitive format. They are composed of individual bits which are, at the next highest level of organization, divided into 10-bit words which are in turn divided into pixels. A series of pixels comprises a line, a series of lines makes up a field, and one or more fields are needed to complete the video frame. To sort out this organization, the SMPTE data sends a special sequence known as a Timing Reference Signal (TRS) at the start and end of each line. By detecting this TRS, it allows the receiver to figure out both the word and line alignment for the signal. At the end of each line, there are a couple of extra words inserted which tell the receiver what the line number is. A CRC is also included, so that the receiver will know if it has properly received all of the data in the line. There are a couple of things that can wreak havoc with receivers: DC content and long periods of time with no transitions. Most communications systems have a way to control this. In the case of the SMPTE 292 serial standard (HD-SDI) it is done with a combination of scrambling and encoding the data.

A good deserializer will extract all of this information for you, and present you with what you need. For this application, it consists of the picture data and the timing data. A deserializer such as the LMH0031 will do this for us, presenting the picture data on two 10-bit data busses. The timing data is presented in the form of three digital signals representing H (start of a horizontal line), V (start of a vertical interval), and F (start of Frame). If the raster format is not interlaced, then you can use just H and V because they are the same.

The serial data is brought into the deserializer where it is decoded and descrambled. Then it is analyzed to find the TRSs which allows the deserializer to know how to break the bits into words. The TRSs' are further analyzed to extract the timing information which is encoded and the data is scrambled, it decodes and descrambles, then the framing is determined so that the deserialized data can be properly word aligned. All of this activity is generally done in the deserializer.

Sync Separator & PLL

Although the video world has gone mostly digital, one area where analog is still very common is in the sync-reference signal, which the studio uses to synchronize all of their equipment. The most common reference to use is a video signal which does not include picture information. This will consist of a series of pulses indicating the start of each video line, with a specific pattern that indicates the end of each field or frame. In this block of our genlock circuit, a sync separator circuit extracts H, V, and F (start of a horizontal line, start of a field, and start of a new frame) from the reference signal, and a PLL circuit generates a pixel clock which is synchronous with the reference signal.

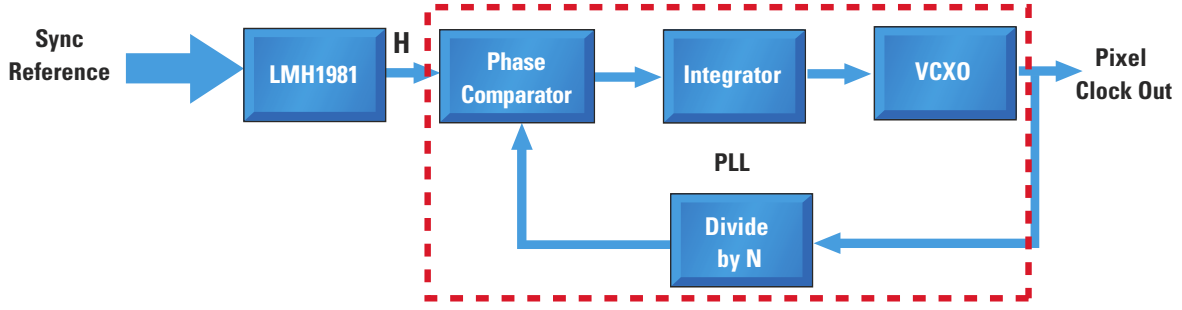


Figure 5. Block Diagram of the LMH1981 Sync Separator & PLL Generating the Pixel Clock

For example, the LMH1981 is a high-performance multi-format sync separator that accepts standard analog SD or HD video signals with either bi-level or tri-level sync. It automatically detects the input video format and applies 50% sync slicing to ensure accurate sync extraction even if the input has irregular amplitude, offset, or noise conditions. To generate the pixel clock, a PLL should be set up to lock to the Hsync output of the LMH1981 and generate the desired clock frequency, which is typically 27 MHz for SD or about 74 MHz for HD. Something to consider when using a PLL for clock generation is that the divide ratio can be quite large and reduce loop bandwidth, which could make the PLL quite sensitive to jitter on Hsync. This makes it especially important to select a sync separator with a very low jitter Hsync output.

Frame Buffer

The frame buffer is simply a block of memory large enough to hold at least one entire frame of the image. This buffer needs to be dual port so that the data coming from the deserializer can be written into one side of the buffer, while data can be read from the other side of the buffer to be fed to the serializer. The buffer is organized in the same way as the video image, with consecutive pixels forming complete lines and consecutive lines forming the complete frame.

Timing Control

The timing control is the heart of the entire genlock system. The basic function is to control the writing into the frame buffer and the reading from the frame buffer. The timing control needs to keep track of two different timing domains. On the input side it receives the data, the timing information, and a clock from the deserializer. This data is written into the frame buffer, with a series of counters that keep track of the pixel and line information. This data is written synchronously with the clock being recovered from the deserializer. At the same time, the timing control takes the timing information coming from the sync separator and the pixel clock. These are used with a second set of counters to read data out of the frame buffer. This data is being read synchronously with the reference sync signal so that the image which was received by the deserializer is now being read synchronously with the reference. The data, along with the pixel clock are fed to the serializer for output. Although video signals have very tight timing specifications, there will be some difference between the input and the output data rates, which means that eventually the frame buffer will either empty out, or overflow. The timing control circuitry has to recognize this situation and periodically repeat a frame or drop a frame to maintain the timing difference between input and output smaller than the size of the frame buffer.

Serializer

Once the data is read out of the frame buffer, it is in parallel format. Before it can be sent to the next piece of equipment it needs to be serialized and formatted to meet the SMPTE 292M HD-SDI standard. From a digital standpoint, new TRS characters are generated and inserted, new line numbers and CRCs are calculated and inserted, the data is then scrambled via the SMPTE scrambling algorithm and converted to NRZI format before being shifted out of a parallel to serial shift register. The key to doing all of this properly is to use a clock clean enough to meet the tight video timing specifications to shift the data out. SMPTE 292M allows no more than 0.2UI of jitter peak-to-peak on the serialized output, which means that the clock jitter needs to be below about 100 ps p-p. Most serializers take a clock which is at the parallel data rate as their input clock (for HD this would be approx 74 MHz) and then multiply it up to the serial rate of 1.5 GHz. Most good serializers will use a PLL for this multiplication that will reject some of the jitter in the original parallel clock. However, for the best performance it is best to start with the cleanest clock possible. In the example sync separator/clock generation circuit, you generated a pixel clock with a VCXO that has very low jitter so that added to the jitter rejection characteristics of the serializer will lead to a very low jitter output. Using the LMH0030 serializer with the VCXO clock source, you could expect your serial jitter to be approx 75 ps, well below the 0.2UI limit.

Summary

Using a handful of simple, off-the-shelf components, you can take a radical input video signal, which is marching to the beat of a different drummer, and get it to straighten up, and march with the rest of our signals. This way, you can switch from one program to another without disrupting the image on your screen. ■

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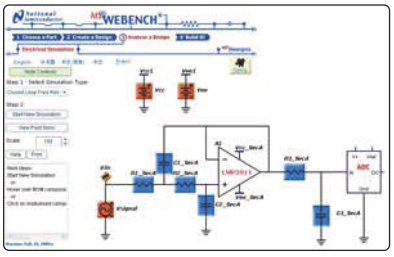

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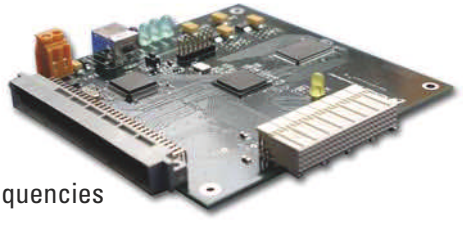

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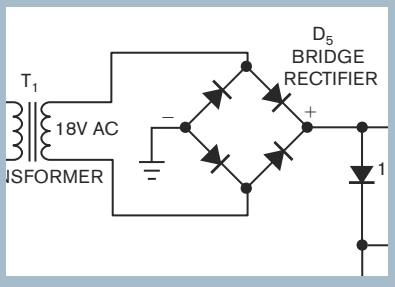

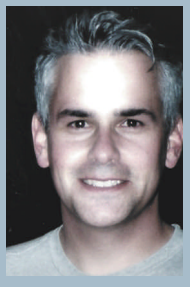

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BY MAURY WRIGHT, EDITOR IN CHIEF

Triple-play roadblocks: technology or competence?

I had the pleasure of writing the cover story in this issue on next-generation broadband technology and how fast broadband links ultimately become the conduit for high-definition video into the home. The research and writing process was like a trip home, as I've followed the topic since the early '90s. Although the technology is fascinating and finally becoming affordable, recent real-life experiences make me wonder whether service providers are sufficiently competent to deliver an error-free triple play.

I first encountered the term "triple play"—delivery of voice, data, and video service over a converged network—around 1992 while doing public relations and technical writing for AT&T Microelectronics, the portion of AT&T that eventually became Agere (www.agere.com). AT&T's Bell Labs had developed both video-codec ICs that made compressed digital video a reality and technologies such as DSL (digital subscriber line) that might deliver such a stream. In fact, AT&T coined the term "switched-digital video" and described a vision close to those that VDSL2 (very-high-bit-rate-DSL) deployments realize today.

AT&T intended to deploy video-on-demand networks within a couple of years. Obviously, the technologists were overly optimistic. It would take more than five years before real DSL and cable deployments offered broadband-Internet-data services. And the triple play has become a reality just in the last few years.

But do the telecom companies and cable MSOs (multiple-service operators) have the competence and discipline to deliver? In North America, the telecom companies certainly understand how to build an ultrareliable network, but they are still struggling with how to compete in an open market and face suddenly unprofitable legacy networks. The MSOs have never really nailed customer service, and they are now offering must-work phone service.

I recently had a very trying experience with Cox Communications (www.cox.com). I have had cable-Internet service from Cox since the late '90s when the company first rolled out the network. DSL was not yet available in my neighborhood, and the cable service has been remarkably reliable since the day Cox installed it. But I've relied on DirecTV (www.directv.com) for video since 1996 when the company beat the MSOs to the punch with college-football pay-per-view packages.

Cox has peppered me with digital-TV offers, including HDTV and DVR. I finally decided to give the company a try, mainly because its HD-DVR offer was far cheaper than the one from DirecTV and it would offer the San Diego Padres in HD, as well.

The process went badly from the start. Cox entered data incorrectly in the computer, delaying installation. The company does not allow users to install the service themselves. When the technician arrived, his eyes glazed over when he looked at my video-distribution panel. I basically guided him step by step.

Well, the digital set-top box worked for about 10 minutes after the tech left. The tech also failed to remove the filter on the analog service to allow analog reception of an expanded channel set, although subscribing to that expanded service was a requirement for getting the digital service.

I called customer service, which told me that I had to schedule another appointment for the following week. I informed the service rep and a supervisor that Cox should fix the problem that day or just come pick up the equipment. They never called back or showed up.

I had been meaning to call Cox, but it wasn't an appealing thought, given the time on the phone that I knew it would require. Meanwhile, my bill arrived with nearly $300 in charges for installation and services.

I just once again did my "phone-jail time" with a customer-service rep. She was nice enough to say that she would waive the service charges thus far. Of course, I informed her that I couldn't owe for something Cox never delivered. I've asked the company to remove the gear, but the rep insists that Cox must send a tech to verify my story before taking any action.

It seems that the triple-play competitors have the same disease afflicting mobile-phone carriers. They are quite adept at marketing and sales and nothing else. Here's hoping DirecTV stays focused on its core competence. EDN

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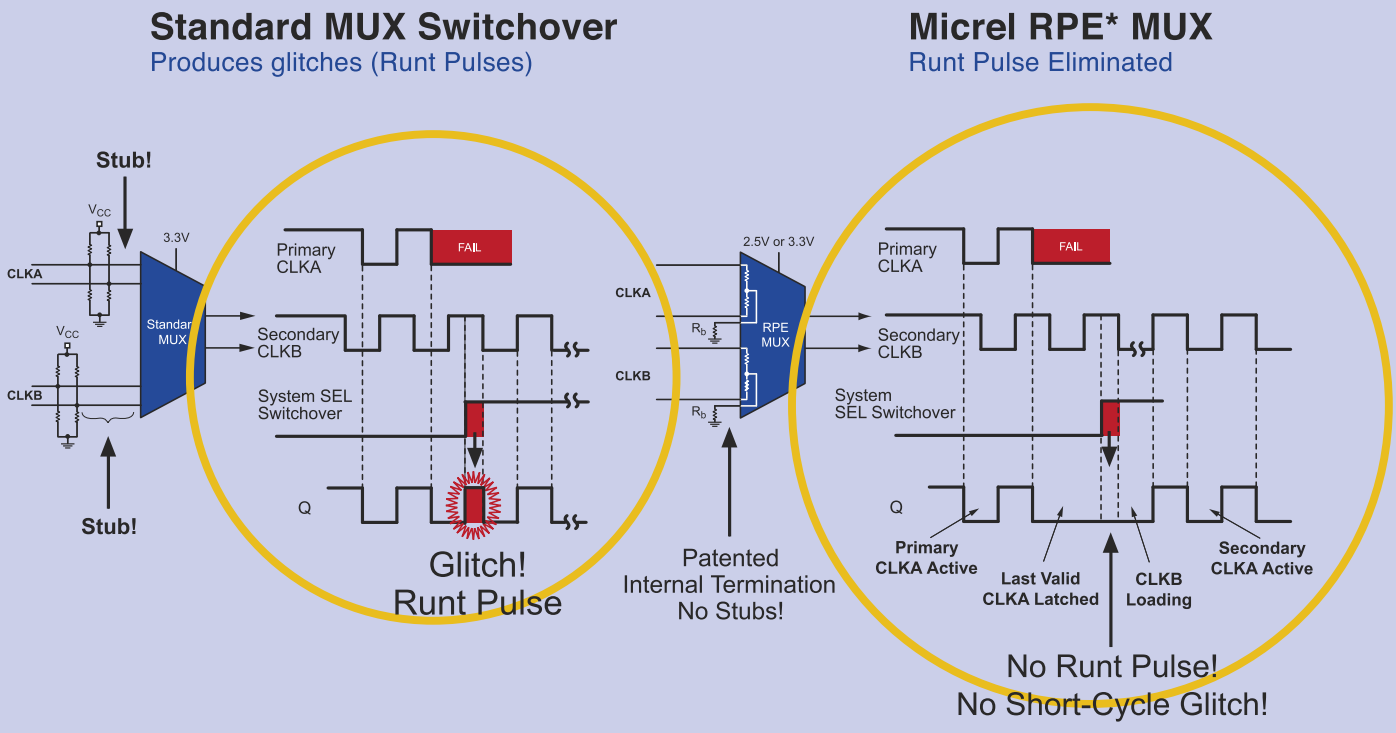

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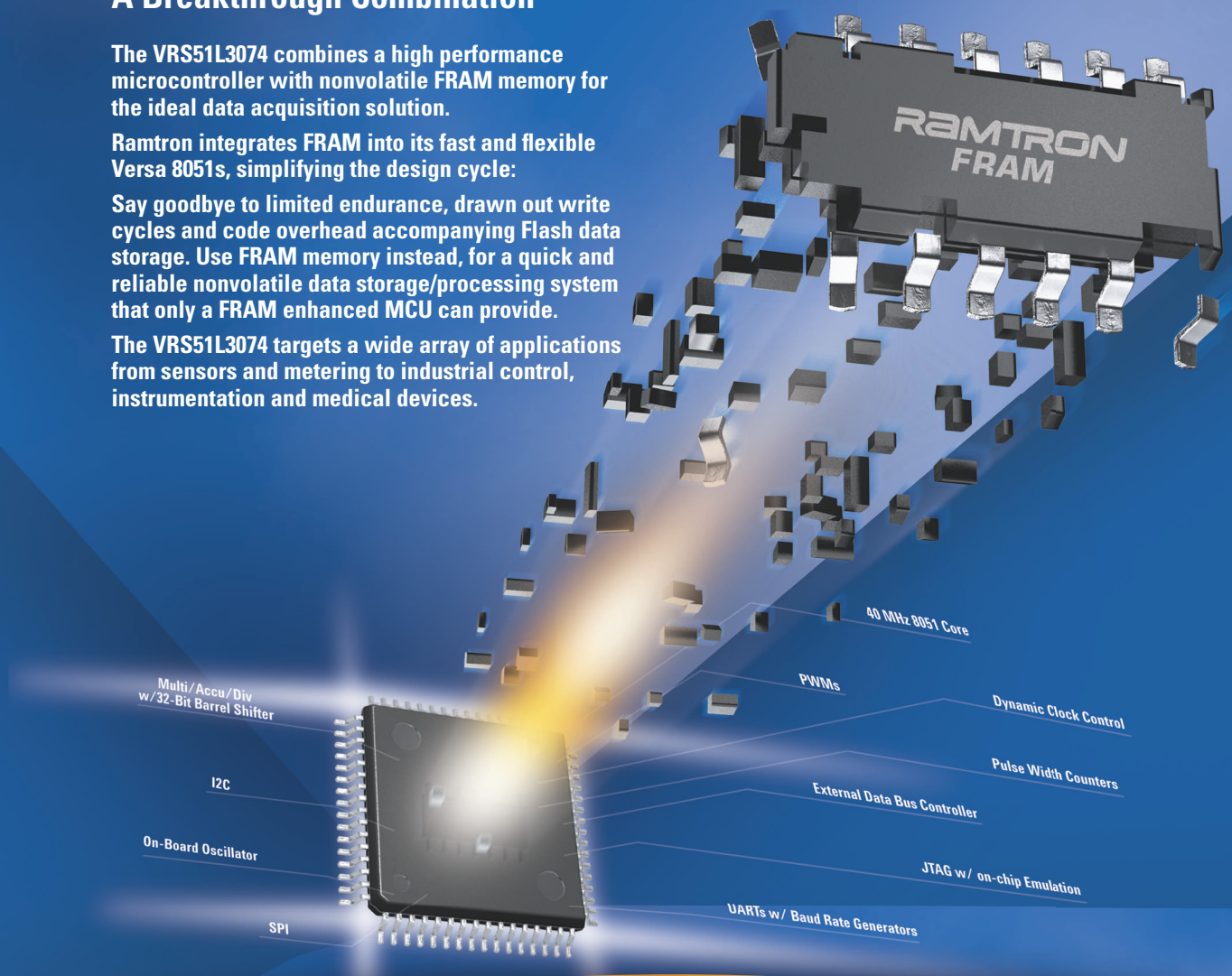

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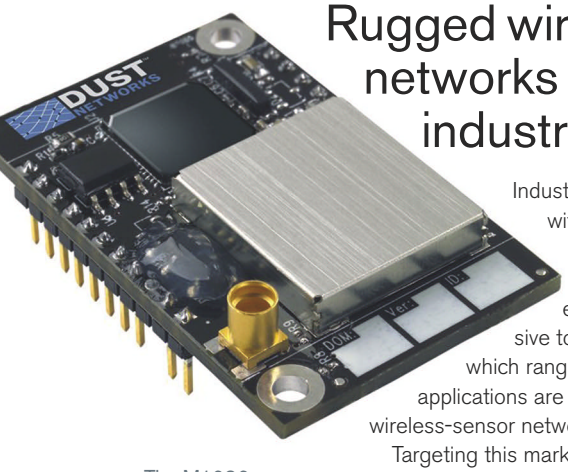


The M1030, an embedded node for the SmartMesh-XT wireless-sensor network, suits harsh industrial environments.

Industrial environments are usually harsh, with hazards such as strong mechanical vibrations, high temperatures, noisy electrical environments, and even explosive gases. It's difficult and expensive to install wiring in these situations, which range from oil rigs to refineries. Thus, these applications are primary targets for ultralow-power wireless-sensor networks.

Targeting this market, Dust Networks has released SmartMesh-XT, an enhancement of its mesh-networking platform. The system offers a rugged design for Class 1 Division 1 environments, including vibration resistance and an industrial-temperature range of −40 to +85°C. The company claims that the network, which relies on the company's TSMP (Time Synchronized Mesh Protocol), achieves reliability greater than 99% in such electrically noisy environments. TSMP, a media-access and networking protocol, operates on standard, off-the-shelf radio chips and allows every node in the mesh network to act as a router.

This product targets use in applications employing the HART (Highway Addressable Remote Transducer) Protocol, which the HART Communication Foundation supports. The protocol, an industrial standard for device communication, calibration, and maintenance, comprises a 4- to 20-mA analog line and a digital signal on the analog line. Rob Conant, Dust's co-founder and vice president of marketing, says, "Most HART devices today don't enable the digital-calibration data because you have to superimpose the digital data on the analog line and go through the distributed-control system." He claims that, by using a separate wireless network to handle the digital diagnostic and calibration data, HART enables you to handle data in parallel rather than intermingling with mission-critical control signals. He says that 25 million HART devices are in use and that most don't enable digital-calibration data.

The family of products comprises network nodes and managers in both the 900-MHz and the 2.4-GHz bands. The 900-MHz products include the M1030 "mote," or node, and the PM1230 embedded-system manager. The 2.4-GHz products, which use IEEE 802.15.4 radios, include the M2135 mote and the PM2130 embedded-system manager. The communication distances for the networks range from 75 to 300m.**—by Margery Conner**

▷**Dust Networks**, www.dustnetworks.com.

Micron jumps into hybrid NANDs

With hybrid-NAND pioneers Samsung (www.samsung.com) and M-Systems (www.m-systems.com) feuding, Micron Technology is seizing the opportunity to introduce a hybrid-NAND device targeting the high-end-cell-phone market. M-Systems and Samsung offer the MDOC (disk on chip) and OneNAND, respectively, which allow designers to boot cell phones using a NAND-based device. Doing so eliminates the need for a NOR device and the extra chip that device involves and adds the capacity and write-speed advantage of NAND. Micron calls its offering the Managed NAND. Like MDOC, Managed NAND pairs a flash die with a microcontroller on a single MCM (multichip module), allowing the company to swap out NAND as higher density NAND becomes available. In contrast, Samsung's monolithic OneNAND device is an SOC (system on chip).

Bob Leibowitz, Micron's NAND-product-marketing director, claims that the Managed NAND is easier to design into wireless handsets than are competing products. He says that, whereas legacy hybrid devices require a design-in, using Managed NAND is akin to qualifying a hard drive for your design because MCM connects to the MMC (multimedia-card) port on wireless processors. The Managed NAND devices have data-transfer rates as high as 52 Mbytes/sec and come in voltages of 1.8V with 1.8V I/O or 3.3V with 3.3 or 1.8V I/O in single-level- or multilevel-cell technology. The product is currently available for sampling and should enter mass production in 2007.

—by Michael Santarini

▷**Micron Technology**, www.micron.com.

C-synthesis tool adds features, capacity

Mentor Graphics has introduced a higher capacity version of its Catapult C ANSI-C++-based synthesis tool that designers can now use to build a prototype of a full DSP-based subsystem. Mentor in 2004 introduced the first version of its Catapult C tool to help IC architects design DSP-centric SOC (system-on-chip) blocks at an algorithmic level. Unlike other ESL (electronic-system-level)-design tools that run on specialized languages, the Catapult C tool uses ANSI-C++ as an input and generates RTL (register-transfer-level) design for hardware design, as well as a SystemC transaction-level model for simulation.

"The source description is strictly functional," says Shawn McCloud, Catapult's product-marketing manager. The source description requires no hardware detail, he claims. Instead, the synthesis tool inserts the hardware detail. "This separation of technological intent from functional specification is a key driver of the technology," says McCloud.

Since its formal introduction in 2004, Catapult C has seen the highest adoption rate of any Mentor tool, he claims, growing 145% in 2005 over 2004. It has seen its highest adoption in Japan. That version of the tool suited only block-level synthesis. The new version of the tool, Catapult SL (system level) adds support for hierarchy and other features that allow architects to use the tool to design a subsystem prototype. The company added a new hierarchical engine that increases the tool's capacity and manages complexity. "Like any other tool in this area, the older version of Catapult synthesized individual blocks. Users would then have to stitch the blocks together," says McCloud. Catapult SL can now do multilevel subsystems.

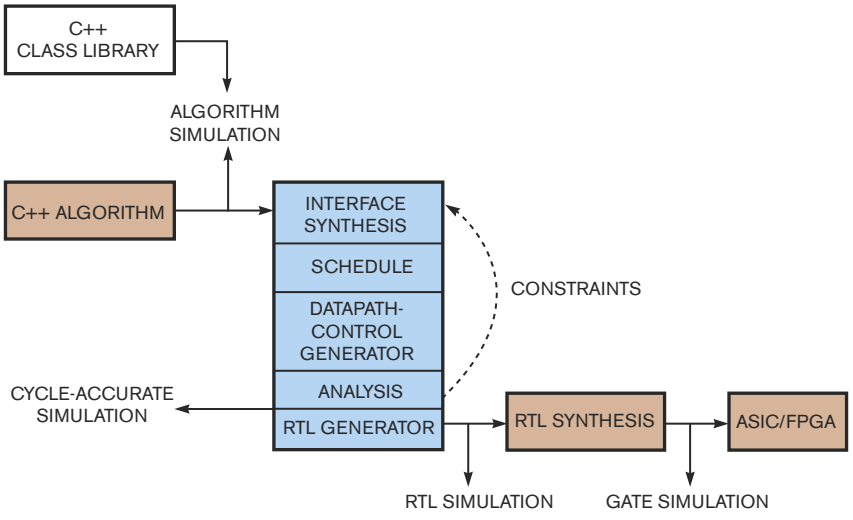
McCloud says that customers have used the SL tool to design 3.5 million-gate subsystems. However, the company believes that the tool can handle 10 million or more gates. The algorithm performs a top-level analysis, propagates all that information to the lower level blocks, and then independently optimizes each block. The tool can reorganize sequential functions to make them run concurrently. A new channel-synthesis feature optimizes the interfaces between the blocks in the subsystem. "It automatically does the analysis of the data rates between the blocks and then automatically inserts the appropriate channel size, FIFO depth, or memory depth to prevent the system from locking when you pipeline the subsystem," McCloud says. Thus, channel synthesis coordinates the communications between the blocks.

The tool can also automatically implement carry-save-adder trees in one step and can generate a SystemC TLM (transaction-level model) that you can feed into Mentor's Questa multilanguage simulator. That tool can generate VCD (value-change-dump) files that you can feed into third-party power tools and then return to Catapult SL to analyze power consumption.

With the introduction of Catapult SL, Mentor has changed the naming convention of its entire Catapult lineup. The original version of Catapult C++ is now Catapult BL (block level) and costs $140,000 for an annual license. The company also offers the ANSI C++ Catapult LB (library builder). Catapult SL costs $350,000 for an annual subscription.

—by Michael Santarini

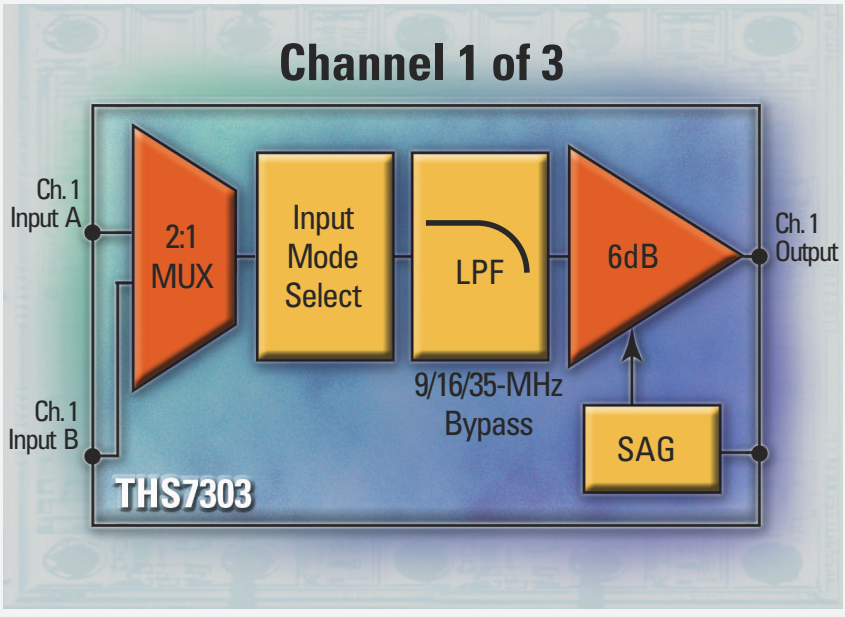
▷**Mentor Graphics**, www.mentor.com.



You can use the Catapult SL tool to design DSP-centric SOC blocks.

DILBERT *By Scott Adams*

3-Ch. Low-Power Video Amp with I²C Control



▶ Applications

- Set-top boxes
- Digital televisions
- Personal video/DVD recorders
- Portable USB devices

▶ Features

- 2.7V to 5V single-supply operation
- Low power consumption: 55mW at 3.3V
- 2:1 Input MUX allows multiple input sources
- I²C Control of all functions
- Integrated low-pass filters with 5th-order Butterworth characteristics
- Selectable input coupling modes
- Rail-to-rail outputs allow a variety of AC- or DC-coupled modes
- Individual channel disable with independent channel mute control

The **THS73x3** family of high-performance video amplifiers from Texas Instruments provides the designer with unprecedented flexibility and control in configuring video systems without the need for hardware upgrades or modifications. Operating at 20x less power than competing amplifiers, these products are ideally suited for digital video systems like those incorporating TI's DaVinci™ and DLP® technologies.

Device	# of Channels	Filter -3 dB Freq (MHz) (typ)	# of Filter Poles	Bypass Bandwidth (MHz) (typ)	Gain (dB)	Input Coupling	Output Coupling	SAG Output	Price Starts at 1K
THS7303	3	9, 16, 35	5	190	6	AC-Bias, AC-STC, DC, DC+Shift	AC or DC	Yes	$1.65
THS7313	3	8	5	–	6	AC-Bias, AC-STC, DC, DC+Shift	AC or DC	Yes	$1.20
THS7353	3	9, 16, 35	5	150	0, Adjustable	AC-Bias, AC-STC, DC, DC+Shift	AC or DC	No	$1.65

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TEXAS INSTRUMENTS

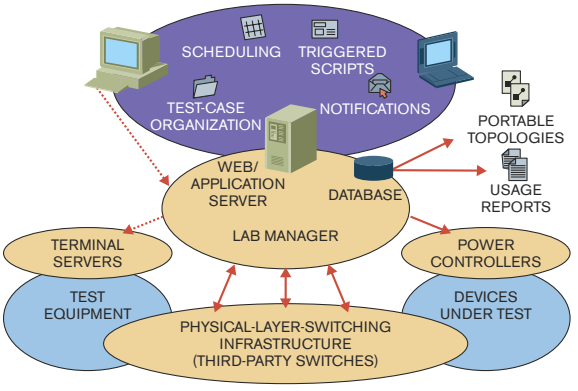
Software optimizes networked-instrument usage

EdenTree Technologies has announced Lab Manager 5.0, a re-engineered version of its award-winning network-lab-automation software. The Lab Manager open-lab operating system works with any kind of network equipment, managing the physical-layer infrastructure to which test equipment and devices under test connect. The result is a software-controlled lab environment with a drag-and-drop user interface that allows engineers to easily and remotely design and implement topologies. The software schedules topologies, configurations, and test scripts; searches for available devices; and reports on device usage. Because it supports a wide range of switches, Lab Manager works in any lab with any devices and any interface types, including POTS (plain-old telephone service)/analog, any rate of Ethernet, optical, Fibre Channel, and RF/coaxial interfaces.

A key reason that labs use the package is to share expensive test equipment among multiple users and multiple test beds. The queue-based scheduler enhances this capability by queuing tests to run as soon as equipment becomes available. Administrators can adjust the priorities or insert higher priority projects into the queue. Another new feature is integration with power controllers, allowing test engineers to control power cycling and system rebooting directly from the GUI. In addition, test engineers can write scripts to control test topologies. Flexible user- and group-level-access permissions allow customers and partners to participate in testing and enable the lab to control its test beds.

Users typically implement Lab Manager 5.0 with their switching infrastructure; list price is $100 per managed port.**—by Dan Strassberg**

▷**EdenTree Technologies**, www.edentreetech.com.



Lab Manager 5.0 coordinates, automates, and simplifies the scheduling of virtually any type of networked lab resources.

Toshiba spins 200-Gbyte, 2.5-in. hard-disk drive

As digital video continues to expand in scope and volume, consumers continue to pile up large data files that—like those dust-gathering VHS cassettes—they are unwilling to delete. Without a viable backup medium for such data volumes, the demand for hard-disk-drive-storage capacity continues to climb for any category of device that is likely to have video on it. Consequently, portable media players and notebook computers are beginning to drive the areal-density curve in the hard-drive market.

The move started with the Apple (www.apple.com) Video iPod and similar devices. Physical constraints dictated a 1- or 1.8-in., low-profile hard-disk drive, but storage demands quickly exceeded the capabilities of conventional lateral recording. The drive industry's next big idea, PMR (perpendicular magnetic recording), began to first appear in tiny drives. For example, Toshiba's storage-device division introduced PMR to its product line in a 1.8-in. drive for media players. The advantage of PMR is its ability to record with the magnetic lines of flux entering the medium vertically rather than laterally across its surface, providing the same volume of magnetic dipoles in a smaller surface area. Hence, the technology provides higher potential areal density for the same SNR. Manufacturers still need to address increasing the recording-signal frequency or slowing the platter to get more bits per millimeter along the track, and moving the tracks closer together.

To get the magnetic-flux lines vertical, Toshiba designed a tunnel-magnetoresistive recording head. Combining all these technologies—PMR, greater bit frequency and track density, and the new head technology—the company recently announced a 200-Gbyte, dual-platter, 2.5-in. drive. The drive targets high-end notebook applications for serious gamers, video junkies, and packrats. Samples are in qualification at high-end-notebook vendors, and Toshiba expects to begin production shipment in August.

This move will not be a one-shot technological leap, according to the company. Theoretically, the limit on achievable areal density for PMR is approximately 1 Tbit/in.^{2}, compared with the roughly 180 Gbits/in.^{2} on the new drive. Toshiba expects for some time to continue driving media, head design, signal paths, and positioners. So, although terabit density is not imminent, Toshiba could drive the current technology platform to produce 500 Gbytes or more in the 2.5-in. form factor.

—by Ron Wilson

▷**Toshiba**, www.toshiba.com.

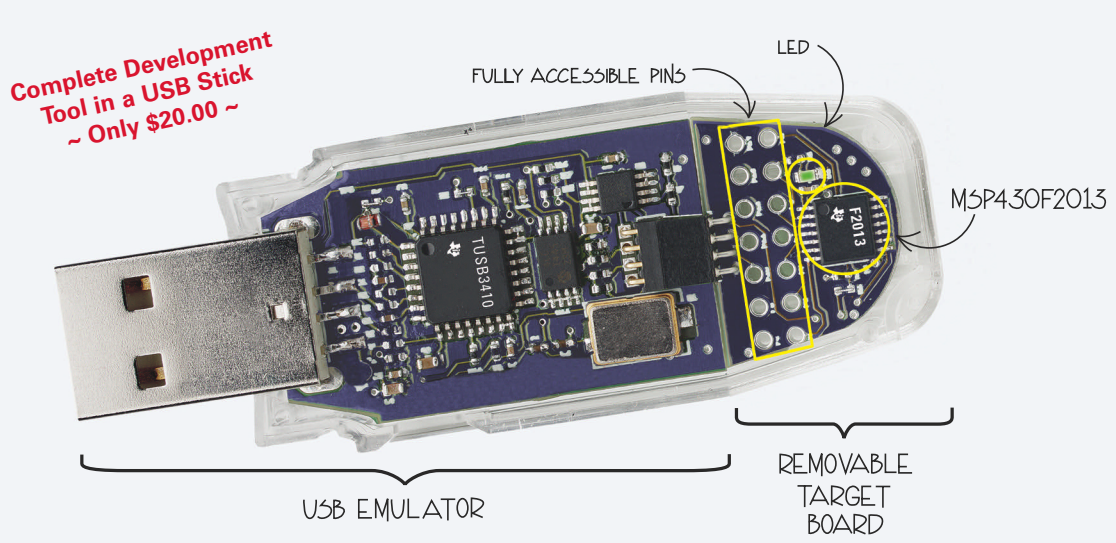
FROM THE VAULT

"'Smaller than a breadbox, 4k words of memory, and less than $10,000.' Remember when that was the definition of a minicomputer? Nowadays, it's not so easy! Today's mini is yesterday's mainframe, and tomorrow's is likely to be today's microcomputer."

Robert Grossman, Senior Editor, and John Conway, Associate Editor, *EDN*, June 5, 1976

MICROCONTROLLERS

Easy.



World's Lowest Power MCU

It's easy to rev up your application in minutes with the new **eZ430-F2013**, the world's smallest complete development tool for only **$20!** The tool provides all hardware and software needed to evaluate the MSP430 or complete an entire F20xx project. The F20xx combines 16 MIPS performance, less than 1 microamp standby current, with your choice of analog converters - from a comparator, fast 10-bit ADC to 16-bit sigma-delta with integrated PGA- all in a package as tiny as 4x4 mm. **Designing with the world's lowest power MCU just got even easier.**

New Low Pin-Count Devices

Device	Program	SRAM	SPI, I²C	Analog	Price 1K USD
MSP430F2001	1 KB	128 B	—	Comparator	$0.55
MSP430F2011	2 KB	128 B	—	Comparator	$0.70
MSP430F2002	1 KB	128 B	✓	10-bit ADC	$0.99
MSP430F2012	2 KB	128 B	✓	10-bit ADC	$1.15
MSP430F2003	1 KB	128 B	✓	16-bit ADC	$1.50
MSP430F2013	2 KB	128 B	✓	16-bit ADC	$1.65

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VOICES

Pat Gelsinger

Whither Intel?

Pat Gelsinger, senior vice president and general manager of Intel's Digital Enterprise Group, recently talked about Intel's future directions, how the company will build on its core competencies, and new processors and who will benefit from them. Excerpts of that interview follow, and you can find the full interview at www.reed-electronics.com/electronicnews/article/CA6329160.

Is innovation leveling off, or is it increasing?

A In some ways, you're seeing clear trends toward less innovation at the chip level because of the cost. What does a 65-nm chip cost? That's why we've seen the number of ASICs declining. At the same time, you're seeing things like FPGAs growing. You take all that together, and there are fewer silicon designs than there were in the past. As we make these architectural transitions to a quad- or eight-core and multicore architectures, we're seeing an acceleration of innovation. I think we were in a period that was boring for a number of years. I see them getting exciting in the future.

It also looks as if other pieces have come a long way, too, so that the integration of all of these technologies can make a much more innovative device.

A I'd agree with that. Innovation is a nonlinear activity. It's not as if Moore's Law is just plunking along and innovation is moving with it. You get to points in which dislocations happen. When Windows happened, it wasn't just as if one day you couldn't do it and then the next day you could. All of a sudden, you had enough excess capacity to change the paradigm of the user interface. We have reached a period in which there's enough excess capacity that you're seeing that next step of innovation. General connectivity is in place across a broad wireless system. There are thin and light form factors. You can start putting a lot of functions into small form factors, and enough computing capacity is left over for your application to become interesting. I do see a cross with high-density memory's changing the memory hierarchy. On the horizon, there are major changes in what we consider a computing device.

Something else seems to have changed here, as well. Intel used to be far more independent. It now seems to be more reliant on a ring of partnerships.

A In many ways, I see that as a skill we've developed. We couldn't do USB. We had to use third-party silicon, we had to facilitate plugfests, and we had to enable the usage-model branding in the industry. We did it with PCI, and we did it with AGPs [accelerated graphics ports]. It's not a new skill, but the scope and the breadth have changed, because now we're trying to facilitate an entire service relationship through broader ecosystem players across global environments. Wi-Fi was a baby step for some of the things we're trying to do now.

Has Intel's core competency changed?

A Some elements of our core competency are unending: underlying process technology; the ability to manufacture in high volume; and sophisticated, high-volume design. That's what we do. Some of these other competencies—we now have thousands of software engineers engaging with service providers, being able to facilitate end-user models—these are things we layer on top of those core competencies. It's pretty far from where we were a decade ago.

Intel is experimenting in a lot of other areas, such as life sciences, too. Where is Intel going with that?

A Our health-care activities fall into three areas. One is IT in institutional health care. How do you accelerate adoption of that? My PC is a lousy form factor when you think of doctors and nurses trying to handle their activities. That's traditional IT in institutional health care. IT penetration in health care around the world is the lowest of any of the major verticals. That is a frightening statement. The second area is personal health care. We have mainframe health care, called hospitals. Now we need the PC version, or personal health care, with connection into the home environment and into self-care.

What's the third area?

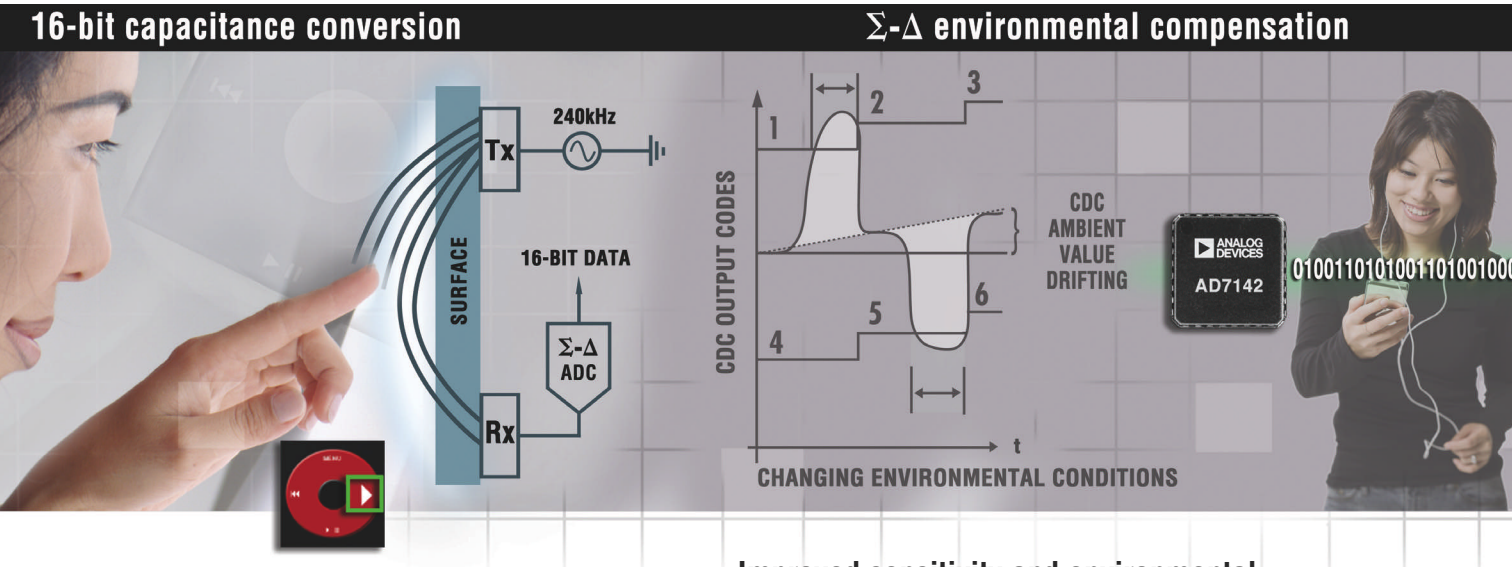
A The things we build at the transistor level are now smaller than all of the components that are the basis of life—proteins, genes, DNA. We can start analyzing at the single-DNA level. This is the deep biological science. We have the world's greatest chemists and physicists and the finest analytical tools on the planet. We added a few biologists, and we're getting great results. We can do a single-DNA analysis or a single-protein analysis. We can detect protein deviations that no one has analyzed before.

But each core is still a processor that deals with ad hoc queries. Haven't those always been a nightmare for multiprocessing systems?

A Yes, and, as a result, we're spending a lot of time looking at workloads, so we can take advantage of those. If everything's a single stream of execution leading to another single stream leading to another, you don't gain a lot of parallelism. Those types of applications are not going to see enormous leaps in capability. At the same time, most of those applications don't need a whole lot of performance. New applications, such as recognition and human interface, mining, and synthesis, have enormous potential for parallelism.

—by Ed Sperling, Editor in Chief, *Electronic News*

16-bit touch controller for the best user experience.
In data conversion, analog is everywhere.

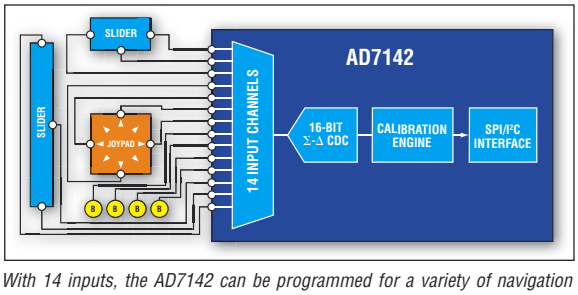


16-bit Σ-Δ CDC …

- <1 femtofarad resolution
- Full power mode: <1 mA
- Low power mode: 50 μA
- Shutdown current: <2 μA
- Supply voltage: 2.6 V to 3.6 V
- Automatic environmental calibration
- Automatic adaptive sensitivity
- SPI® or I²C® interface
- 32-lead 5 mm × 5 mm LFCSP
- Price: $1.65 (1k quantities)

… enabling multiple applications

- Consumer electronics
- Medical instrumentation
- Automotive applications
- Industrial equipment
- PC peripherals



With 14 inputs, the AD7142 can be programmed for a variety of navigation functions including buttons, sliders, scroll wheels, and joypads.

Improved sensitivity and environmental calibration—made possible by Σ-Δ conversion

For products with increasing feature convergence, finger-driven navigation enhances the user experience—for designers as well as consumers. The AD7142 capacitance-to-digital converter (CDC) with on-chip environmental compensation delivers unmatched touch control performance. It offers:

- Reliable performance over supply and temperature
- Programmable functionality and touch sensitivity
- 50% lower power than competitive solutions
- Development tools, such as reference designs and host software, that reduce time to market

ADI also offers CDC solutions for measuring proximity, position, level, pressure, and humidity.

New online seminar:
View the "Innovative Human Interface Design Techniques Using CDCs" seminar at *www.analog.com/onlineseminar-CDC*.

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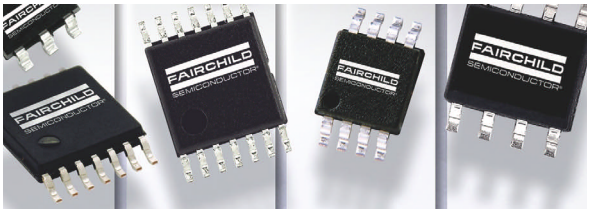
ANALOG DEVICES



The FHP3x50 family targets HD video.

GLOBAL DESIGNER

Video op amps exceed HD needs

The most recent incarnation of power-semiconductor supplier Fairchild Semiconductor brands itself the "power franchise." Now, discrete supplier Fairchild is re-entering the high-performance-op-amp arena with the FHP3x50 voltage-feedback-amplifier family for use in HD (high-definition) video products, such as set-top boxes. These amplifiers for video-signal chains address a market in which the company provides components such as video-filter drivers. Fairchild bases these parts on the new low-capacitance, complementary-bipolar-silicon-on-insulator BCP-6T process. Company officials claim that the process enables the amplifiers to deliver higher bandwidth, more output current, and better dc performance than competing products.

The FHP3x50's full-power bandwidth is 210 MHz at −3 dB, and the chips have a 1100V/μsec slew rate and 0.07%/0.03° differential gain and phase error. Gain flatness of 0.1 dB extends to 50 MHz, and Fairchild officials say that pulse response is good with fast slewing edges and minimal preshoot, undershoot, or overshoot. Input-bias current is 0.05 mA, and the devices use 3.6 mA. Output-drive capability is ±55 mA. The chips are available in triple and quad packages.

For standard-definition systems, the fast rail-to-rail amplifiers of the FHP3x30 family come as singles, duals, and quads and offer unity-gain bandwidth of 170 MHz, driving ±100-mA outputs.

Fairchild also claims competitive advantages in gain/phase error, gain flatness, and pulse response over other devices of the same class. These devices suit use in video-signal chains and also work as general-purpose amplifiers. Prices range from 49 to 86 cents (1000).

—by Graham Prophet, *EDN Europe*

▷**Fairchild Semiconductor**, www.fairchildsemi.com.

LEDs take over in "mood" lighting

Using tricolor arrays of LEDs, architects and lighting designers can fine-tune intensity, color, and pattern to achieve "mood" lighting and other effects. Designers need to ensure that they apply the correct drive to the LEDs, and they need to program the desired patterns into LED arrays.

For both groups of designers, distribution company EBV has developed a reference design and demonstration board that mounts a 5×5-unit array of tricolor LEDs on a pc board that acts as a "tile," allowing designers to build an effects-lighting panel of any size. The pc board measures 76×76 mm and is populated with 25 Osram (www.osram-os.com) RGB LEDs. To individually drive each diode for full control of effects requires 75 PWM channels, which EBV has implemented in an Altera (www.altera.com) MAX II EPM 1270 CPLD. The MAX II chip suits this application, because each of its I/O pins can sink as much as 25 mA and can, therefore, directly drive the LEDs.

The logic on the CPLD implements the PWM channels, handles the communications, and decodes the incoming data into control signals for each LED. For demonstration purposes, the board integrates an RGB color generator to show a rainbow effect running over the array. Two RS-485 channels and one RS-232 input channel allow you to feed external patterns to the pc board. EBV can also provide a graphics-effects-controller board that its partner company, ecue (www.ecue.tv), designed, along with software to create lighting effects and patterns of the designer's choice. The DBMAXLED board comes as a kit for €250 (approximately $315).

—by Graham Prophet, *EDN Europe*

▷**EBV Elektronik**, www.ebv.com.

I²C bus now runs at 1 MHz

07.06.06

Chip designers use the two-wire, serial I²C bus for a range of interchip communications. Philips, which originated the bus more than 20 years ago, has now announced Fm+ (fast-mode-plus) devices that take the performance of the I²C bus up to 1 MHz. Previous increments in the speed of the bus include the 400-kHz standard and fast modes. Devices that exploit the performance that Fm+ offers include LED controllers and chips dedicated to stand-alone-bus-driving functions.

The four-color PCA9633 LED driver and controller for color-mixing applications features four controllers for the LED outputs and a fifth to simultaneously dim or blink all the LEDs. The chip has 4-bit level control and responds to four addresses, increasing the flexibility that programmers can use when creating lighting effects. Users can operate as many as 126 devices on the same bus without bus extenders.

Two other devices perform 40-bit I/O expansion. With the PCA9698, you can support as many as 64 nodes on the same bus. Features include 40 I/O pins with configurable outputs; output states that you can switch using acknowledge or stop commands; non-interrupt-generating, maskable interrupts; a hardware-output enable; and an SMBusAlert function. The parallel-to-I²C PCA9665 controller drives buses having as much as 4-nF capacitance. You can use a standard microcontroller as an Fm+ bus master, and the device includes a 68-byte buffer to simplify programming.—by Graham Prophet, *EDN Europe*

▶**Philips**, www.philips.com.

LEADING inside

A series of engineering insights
by Analog Devices.

Data and Power Isolation in One Package Provides Total Isolation Solution

A common challenge in designing systems that require galvanic isolation is finding a cost-effective, space-efficient way to isolate both power and data. While many commercially available solutions exist for isolating data, isolating power often requires the unsatisfactory choice between designing a custom, isolated supply or using costly discrete isolated dc-to-dc converters. This challenge arises because traditional isolators, such as optocouplers, can isolate data but cannot generate power, whereas transformers can isolate power but are neither space nor cost-effective for isolating most data channels.

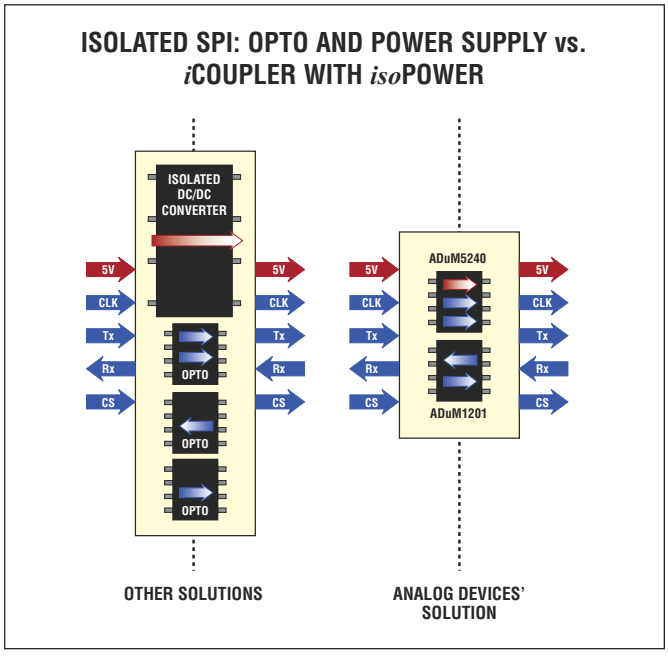
Custom isolated supplies can be cost-effective at high volumes, and they can deliver just the right level of performance for the given application. However, they require both design expertise and separate safety approvals, which add development time and cost. The second option, discrete isolated dc-to-dc converters reduce development time and consume less space; however, they are often more than twice the cost of custom supplies, and they have limited isolation ratings.

Analog Devices *i*Coupler® products with *iso*Power™ technology offer a new approach that greatly reduces size and cost without compromising on data rate and isolation rating. It starts with *i*Coupler digital isolators that employ chip scale microtransformers in contrast to LEDs and photodiodes used in optocouplers. Compared to optocouplers, *i*Coupler products consume less power, achieve higher data rates and provide more precise timing; yet still provide isolation ratings of up to 5 kV. With the introduction of *i*Coupler technology more than five years ago, safe, reliable data transfer has been provided by over 50 million channels of digital isolation.

The same transformers in these devices can be used to make an isolated dc-to-dc converter, creating a total isolation solution in one surface-mount package. Using Analog Devices' *iso*Power technology, a new family of devices integrates 50 mW of isolated power and two 10 Mbps data channels with 2.5 kV isolation, providing a total solution in one package.

Analog Devices' ADuM524x products provide galvanic isolation by transmitting data across an isolated transformer, using integrated CMOS electronics for signal conditioning. The same chip scale transformers are used to generate isolated power, but the CMOS electronics drive the primary side, and then rectify and regulate the supply on the isolated secondary side. The resulting internal dc-to-dc converter supplies power to the isolated side of the ADuM524x and makes available up to 10 mA of current at 5 V for use in a variety of applications.

The figure below compares SPI buses that are isolated by optocouplers and a discrete dc-to-dc converter with Analog Devices' solution that uses one ADuM5240 dual-channel *i*Coupler with *iso*Power and one ADuM1201 dual-channel *i*Coupler. The Analog Devices' solution reduces solution size and cost by more than 50%.



Analog Devices' solution reduces size and cost by over 50%.

The ADuM524x *i*Coupler products with *iso*Power technology, available in 8-lead SOIC packages and priced at $2.95 per unit in 1k quantity, provide a simple, low cost, space-saving isolation solution. In addition, Analog Devices offers a wide range of 2.5 kV standard isolators, and the ADuM240x family of 5 kV quad-channel isolators, plus a range of application focused devices, for example, the ADuM1230 isolated gate driver. For datasheets, free samples, and more information, visit *www.analog.com/iCoupler-tech.*

Author Profile: ***David Krakauer*** *is marketing manager for Analog Devices' i*Coupler *product line.*

BY BONNIE BAKER

When is good enough good enough?

If you are having difficulty making product-selection decisions in a consumer circuit, such as the temperature-sensor circuit in **Figure 1**, you can quickly solve this problem by choosing the absolute best performing parts for each socket. Is this statement true or false? Using this type of logic may give you a confident feeling that your circuit will work correctly the first time. However, following such logic goes only so far when you try to justify the cost-versus-performance factors of the products you are using.

In **Figure 1**, note that a 12-bit converter is at the end of the signal chain. So, are the highest performance analog products in front of the ADC appropriate? How do you determine which products are good enough for your system? Avoiding production-floor notifications or field failures may be your definition of "good enough."

Instead of choosing the best products, you can use the RSS (root-sum-square) algebraic approach. One criterion is to keep the signal within the dynamic range of the full-scale range of the ADC. The product characteristics that influence the extent of the dynamic range are the system's cumulative offset and gain errors.

As an example, assume that the maximum offset error of IC_1 and IC_2 is 0.5 mV. The offset error of the ADC is ±1 LSB or ±1.22 mV. (The full-scale range of the ADC is 5V.) The gain error of both the sensor cell and the IC_1 amplifier configuration depends on the ±1% maximum resistor tolerances as well as on a maximum sensor-resistor tolerance of ±2%. The ADC's contributed gain error is 0.098% or equals 4.9 mV maximum at full scale.

To determine the dynamic-range limitations of the circuit, if you combine all of these terms, you would calculate the combined RSS value of offset and gain, bringing these errors to the ADC's input. With the RSS formula, you take the square root of the sum of the squares of several terms that are statistically independent. You cannot use an RSS formula with entities that have correlated variations that are not statistically independent.

For instance, the worst-case sensor-resistive offset error would be ±94 mV×10V/V. The contribution of the amplifier-gain stage, IC_1, is ±500 μV×10, the filter-stage (IC_2) offset error is ±500 μV, and the ADC (IC_3) offset error is ±1.22 mV. The cumulative possible offset error at the ADC's input is $\sqrt{(sensor^2+IC_1^2+IC_2^2+IC_3^2)}=940$ mV. This calculation illustrates that the sensor cell contributes the most error with little impact from the amplifiers or the ADC. Using the same logic, you would use the RSS formula to determine gain-error contribution that limits the dynamic range from the four stages in this circuit.

So, during your first consumer-product-selection attempt, you can use RSS calculations. These calculations can assist you in making logical and economical product decisions. Once you take this first step, make sure you use the same evaluation technique in your manufacturing process to quantify the effects of the processes—such as solder reflow—that you impose on these devices and the end-of-life effects due to environmental exposures. EDN

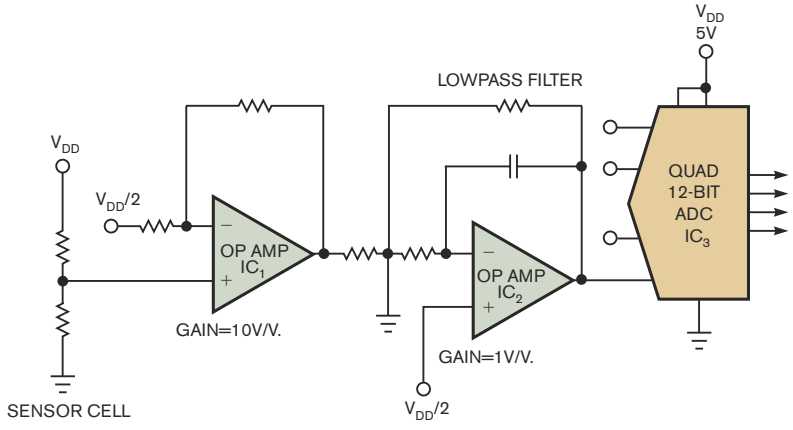


Figure 1 In this typical 12-bit temperature-sensing circuit for consumer applications, the gain of IC_1 is 10V/V, and the gain of IC_2 is 1V/V.

REFERENCE

1 Sandler, Steven M, "A Comparison of Tolerance Analysis Methods," AEi Systems LLC, 1998, www.ema-eda.com/products/other/articles/Tolerance_Methods.pdf.

Bonnie Baker is a senior applications engineer at Texas Instruments and author of A Baker's Dozen: Real Analog Solutions for Digital Designers. *You can reach her at bonnie@ti.com.*

Texas Instruments

INTERFACE

Analog Applications Journal

BRIEF

Device spacing on RS-485 buses

By Kevin Gingerich • *High-Performance Linear/Interface*

Introduction

The RS-485 bus is a distributed parameter circuit whose electrical characteristics and responses are primarily defined by the distributed inductance and capacitance* along the physical media. The media is defined here as the interconnecting cable(s) or conducting paths, connectors, terminators, and RS-485 devices added along the bus. The following analysis derives a guideline for the amount of capacitance and its spacing that can be added to the bus.

For a starting approximation, the characteristic transmission line impedance at any cut point in the unloaded RS-485 bus is defined by the following equation, where L is the inductance per unit length and C is the capacitance per unit length.

$$Z = \sqrt{\frac{L}{C}}$$

As capacitance is added to the bus in the form of devices and their interconnections, the bus impedance is lowered to Z′, causing an impedance mismatch between the media and the loaded section of the bus.

As the input signal wave arrives at this mismatch in impedance, an attenuation (or amplification) of the signal will occur. The signal voltage at an impedance mismatch is $V_{L1} = V_{L0} + V_{J1} + V_{R1}$, where V_{L0} is the initial voltage, V_{J1} is the input signal voltage, and V_{R1} is the reflected voltage. The voltage reflected back from the mismatch is $V_{R1} = \rho_L \times V_{J1}$, where

$$\rho_L = \frac{Z' - Z}{Z' + Z}$$

and is the coefficient of reflection commonly used in transmission line analysis. The voltage equation can now be written as $V_{L1} = V_{L0} + V_{J1} + \rho_L \times V_{J1}$.

With fast transfer rates and electrically long** media, it becomes essential to achieve a valid input voltage level on the *first* signal transition from an output driver anywhere on the bus. This is called incident-wave switching. If incident-wave conditions are not achieved, reflected-wave switching must be used. To achieve a valid logic voltage level, reflected-wave switching depends upon reflected energy occurring some time after the first transition arrives.

Assuming that the bus is terminated at both ends with the nominal media impedance and no fail-safe offset, an RS-485 driver will create a high-to-low voltage change from at least 1.5 V to –1.5 V, or a V_{J1} of –3 V. The signal voltage at the load, V_{L1}, should go below the minimum receiver input voltage threshold of –0.2 V.

$$-0.2 > 1.5 + (-3) + \rho_L \times (-3)$$

$$\rho_L > \frac{-0.2 - 1.5 + 3}{-3} = -0.43$$

Now we can solve for Z′:

$$\rho_L = \frac{Z' - Z_0}{Z' + Z_0} > -0.43$$

$$Z' - Z_0 > -0.43(Z' + Z_0)$$

$$Z'(1 + 0.43) > Z_0(1 - 0.43)$$

$$Z' > 0.4Z_0$$

If the loaded bus impedance is no less than $0.4Z_0$, the minimum threshold level should be achieved on the incident wave under all allowed cases.

What bus configuration rules should be used to keep the loaded bus impedance above $0.4Z_0$?

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* All capacitances are differential in this article. The differential is approximately one-half of the single-ended capacitance.

** "Electrically long" is defined here as $\tau > \frac{t_{10\text{-}90\%}}{3}$

where t is the one-way time delay across the bus and $t_{10\text{-}90\%}$ is the 10% to 90% transition time of the fastest driver output signal.

In the derivation of the minimum loaded-bus impedance, we treat the addition of devices and their capacitances in a distributed model. As such, the loaded-bus impedance can be approximated by

$$Z' = \sqrt{\frac{L}{C + C'}}$$

where C′ is the added capacitance per unit length. If we knew the distributed inductance and capacitance of the media, we could calculate Z′ directly. Unfortunately, manufacturers do not commonly specify these; but they generally do specify the characteristic impedance, Z_0, and the capacitance per unit length, C. With these and the relationship

$$Z_0 = \sqrt{\frac{L}{C}}$$

we can solve for L, as $L = Z_0^2 C$. Then we can substitute into the equation for Z′ and simplify:

$$Z' = \sqrt{\frac{Z_0^2 C}{C + C'}} = Z_0 \sqrt{\frac{C}{C + C'}}$$

C′ is the distributed device capacitance (C_L) divided by the distance (d) between devices:

$$C' = \frac{C_L}{d}$$

Substituting this into the equation, we can solve for d:

$$Z' = Z_0 \sqrt{\frac{C}{C + \frac{C_L}{d}}}$$

$$\left(\frac{Z'}{Z_0}\right)^2 = \frac{C}{C + \frac{C_L}{d}}$$

$$C\left(\frac{Z_0}{Z'}\right)^2 = C + \frac{C_L}{d}$$

$$d = \frac{C_L}{C\left[\left(\frac{Z_0}{Z'}\right)^2 - 1\right]}$$

Now substituting our minimum Z′ of $0.4Z_0$ gives us d in meters (if C is pF/m) or feet (if C is pF/ft):

$$d > \frac{C_L}{C\left[\left(\frac{Z_0}{0.4Z_0}\right)^2 - 1\right]}$$

$$d > \frac{C_L}{5.25C}$$

We now have a relationship for the minimum device spacing as a function of the distributed media and lumped-load capacitance. Figure 1 shows this relationship graphically.

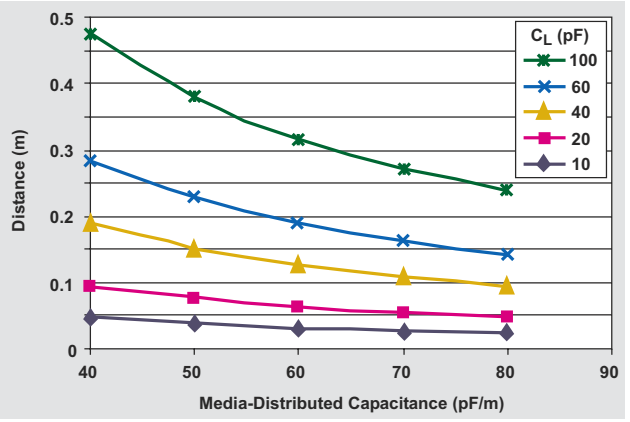


Figure 1: TPS79918 Internal Block Diagram

Load capacitance includes contributions from the RS-485 line circuit bus pins, connector contacts, printed-circuit-board traces, protection devices, and any other physical connections as long as the distance from the bus to the transceiver is electrically short. RS-485 5-V transceivers, such as the SN65HVD1176, have a capacitance of 7 pF. Transceivers with a 3-V supply, such as the SN65HVD11, have about twice the capacitance that 5-V transceivers have at 16 pF. Board traces add about 0.5 to 0.8 pF/cm depending upon their construction. Connector and suppression device capacitance can vary widely. Media-distributed capacitance ranges from 40 pF/m for low-capacitance, unshielded, twisted-pair cable to 70 pF/m for backplanes.

This derivation gives guidelines for spacing of RS-485 nodes along a bus segment based upon the lumped-load capacitance. The method is equally applicable to other multipoint or multidrop buses, such as CAN, RS-422, or M-LVDS, with appropriate adaptation of the parameter values.

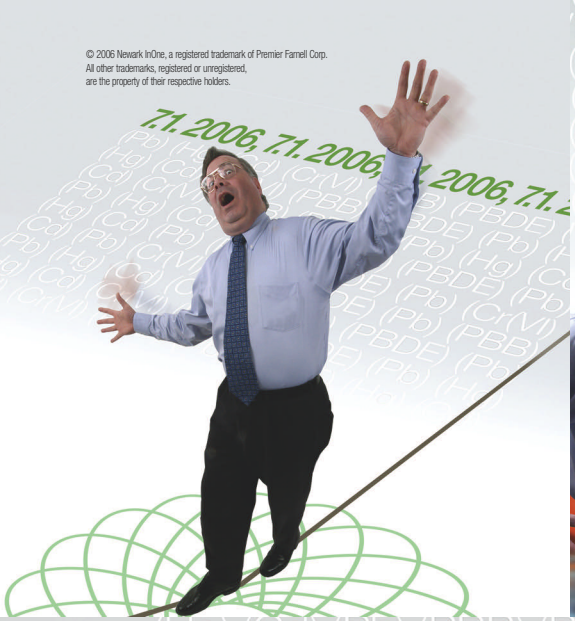
References:

Related Web sites

interface.ti.com

www.ti.com/sc/device/SN65HVD11

www.ti.com/sc/device/SN65HVD1176



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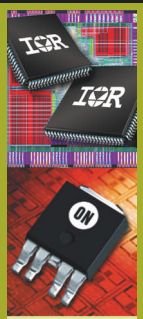

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For expanded analysis and additional internal pictures of the MP3-818, visit www.edn.com/060706pry.

MP3 disassembly: tech for thrifty tune-toters

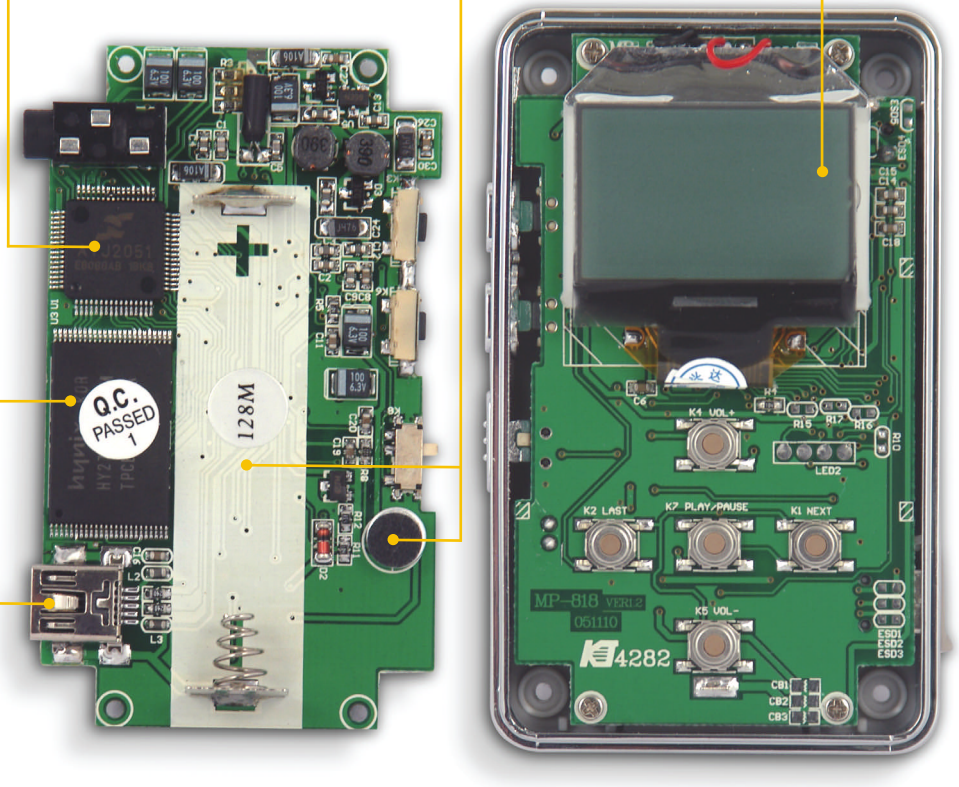
After I bought a laser-printer-toner cartridge, a "free-with-$75-purchase" coupon also brought an OD-128MP3, also known as the MP3-818, portable digital-audio player to my door. The price was music to my ears, especially considering that Office Depot normally lists the player for $69.99. The features aren't too shabby either: MP3- and WMA (Windows Media Audio)-codec support, an LCD (take *that*, iPod Shuffle!), and even voice-recording capability. What's inside the 1.75×3×0.75-in. silver case?

The monochrome LCD is physically distinct from its bright-blue companion backlight; the two devices press together in the assembled MP3-818. The system design is both highly integrated and rugged; it survived my disassembly-and-reassembly sequence with aplomb.

Considering the "made-in-China" moniker on the MP3-818's packaging, I strongly suspected I'd find homegrown silicon inside. I was right: A 24-bit Actions Semiconductor ATJ2051, clocked at 72 MIPS and based on a Z80 core, runs the show. Other members of the ATJ20xx family support multichannel recording, hardware-accelerated real-time MP3 encoding, and enhanced system connectivity.

An AAA-battery bracket dominates one side of the pc board; the microphone is in the bottom right corner.

A 1-Gbit Hynix flash memory is the sole stand-alone memory chip. I presume it holds both the audio files and the firmware image, because the ATJ2051 supports booting from NAND flash memory.



The MP3-818 presents itself as a USB-memory device to a connected PC, enabling you also to store general-purpose files on it. This configuration decision, however, doesn't enable the MP3-818 to support digital-rights-managed WMA files.

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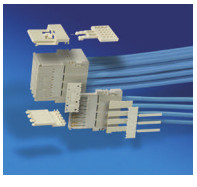

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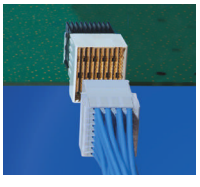

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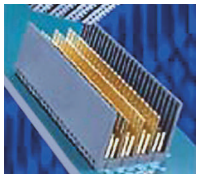

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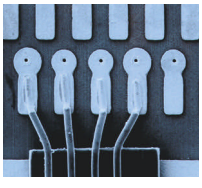

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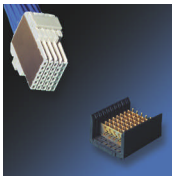

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Is chip design DIFFERENT after 90 nm?

DESIGN TEAMS FIND THAT SUCCESS REQUIRES SOME FUNDAMENTAL CHANGES IN THINKING AND IN TEAM STRUCTURE IN THE 90- AND 65-NM PROCESSES.

At every new process node, IC design becomes more difficult. But, as design teams contemplate the move to 90- and then 65-nm-process nodes, many are asking whether the increased difficulty is still just a matter of degree or whether something fundamental is changing. Does a successful 90-nm-design team differ in some way from a successful 130-nm-design team? If so, is the change a one-time thing, or are the differences even greater at 65 nm? The only way to find out is to talk to successful design teams.

Big differences exist in the degree of complexity between the 90- and 65-nm processes, especially for teams performing cell-based design. A top-level diagram of the 90-nm flow that fabless-ASIC vendor Open-Silicon uses shows new branches (**Figure 1**). Jay Jayaprakash, ASIC-design manager at Open-Silicon, groups the new challenges at the 90-nm-process node into power, signal integrity, DFM (design for manufacturability), and design for test. In the power and signal-integrity areas, increased complexity for the design team is arguably a matter of degree. Power management is more critical at the 90-nm node, and it requires the concerted effort of cell designers, tool designers, logic designers, and architects. But this situation does not fundamentally differ from the situation at the 130-nm node. Higher leakage currents at the smaller node exacerbate the problem. Similarly, signal-integrity analysis is more demanding; teams must use the available tools and pay heed to their results.

In addition, Jayaprakash says, HSpice engineers are becoming more central to the digital-design flow at the 90-nm node. Teams must use Spice for their clock nets—something many have been doing for several generations—and this sort of detailed analysis is also becoming important on critical signal paths. In the signal-path area, you see the first glimmer of the need for new skills involving digital-timing analysis. "STA [static-timing analysis] is ballooning out of control on us," Jayaprakash says. "There are different process corners for different operating modes, and there are different corners for the parasitic-extraction tools that are providing the base data for your STA. By the time you account for all the corners, you are doing 50 or 60 runs, and then what do you do with all the data?"

As STA becomes more complex, some designers are looking at IBM's SSTA (statistical-STA) tool. Instead of running a single STA at each combination of the process and extraction corners, SSTA attempts to express each delay as a probability distribution and then to compose these distributions as they move through the nets to produce outputs that are

AT A GLANCE

- Guardbanding at 90 nm results in chips that are too big or too slow.
- DFM (design-for-manufacturability) tools still cannot accurately predict circuit performance or yield.
- The choice of which rules and guidelines to obey comes down to a judgment call that requires physical-design people to be process-knowledgeable.
- The need for process knowledge is spreading upward to architecture.

themselves statistical distributions. It appears to have many more skeptics than fans among design teams. Part of the skepticism comes from the huge amount of process-related data that is necessary to produce accurate delay distributions in the first place. SSTA may be practical only in an integrated-device manufacturer or a fab-owning ASIC company simply because the tool must work so closely with the process models. But another issue looms even larger in the minds of many designers: What do you do with the output? What does it mean to learn that the timing slack on a net is statistically distributed around −12 psec with a sigma of 24 psec? "We have a tool, but we have to learn what to do with it," observes Riko Radojcic, principal engineer at Qualcomm. "SSTA is a fuzzy world, not a black-and-white one."

The question of statistical timing opens a window—albeit a cloudy one—into the most fundamental changes that are taking place in design teams as they adapt to the 90-nm process. Imagine that a timing engineer asked a process engineer what the delay on a net is. The process engineer might say that the delay depends on the switching speed of the driver transistor. That speed, in turn, depends on the threshold voltage of the transistor, the gate leakage, the effective channel width and length, the drain resistance, and the source and drain contact resistances. Those values vary, depending on the dimensions and shapes of the source and drain implants and the gate polysilicon. They also depend on the shape and composition of the source and drain contacts, which vary considerably in this process. And those things, in turn, depend on the proximity of the transistor's well implants, the density and pitch of the pattern of polysilicon-gate features, and the proximity of corners or width changes in the polysilicon.

After learning about these and a host of other factors, the timing engineer, who

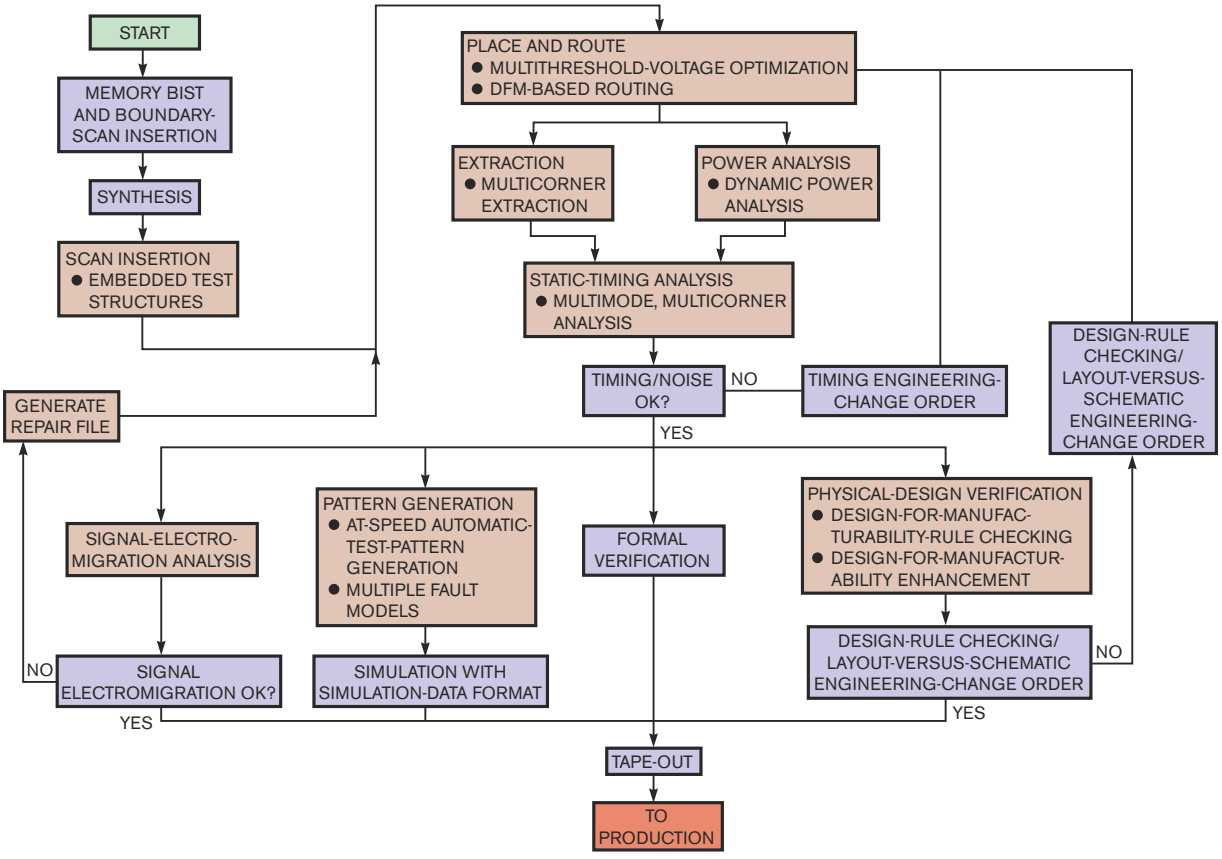
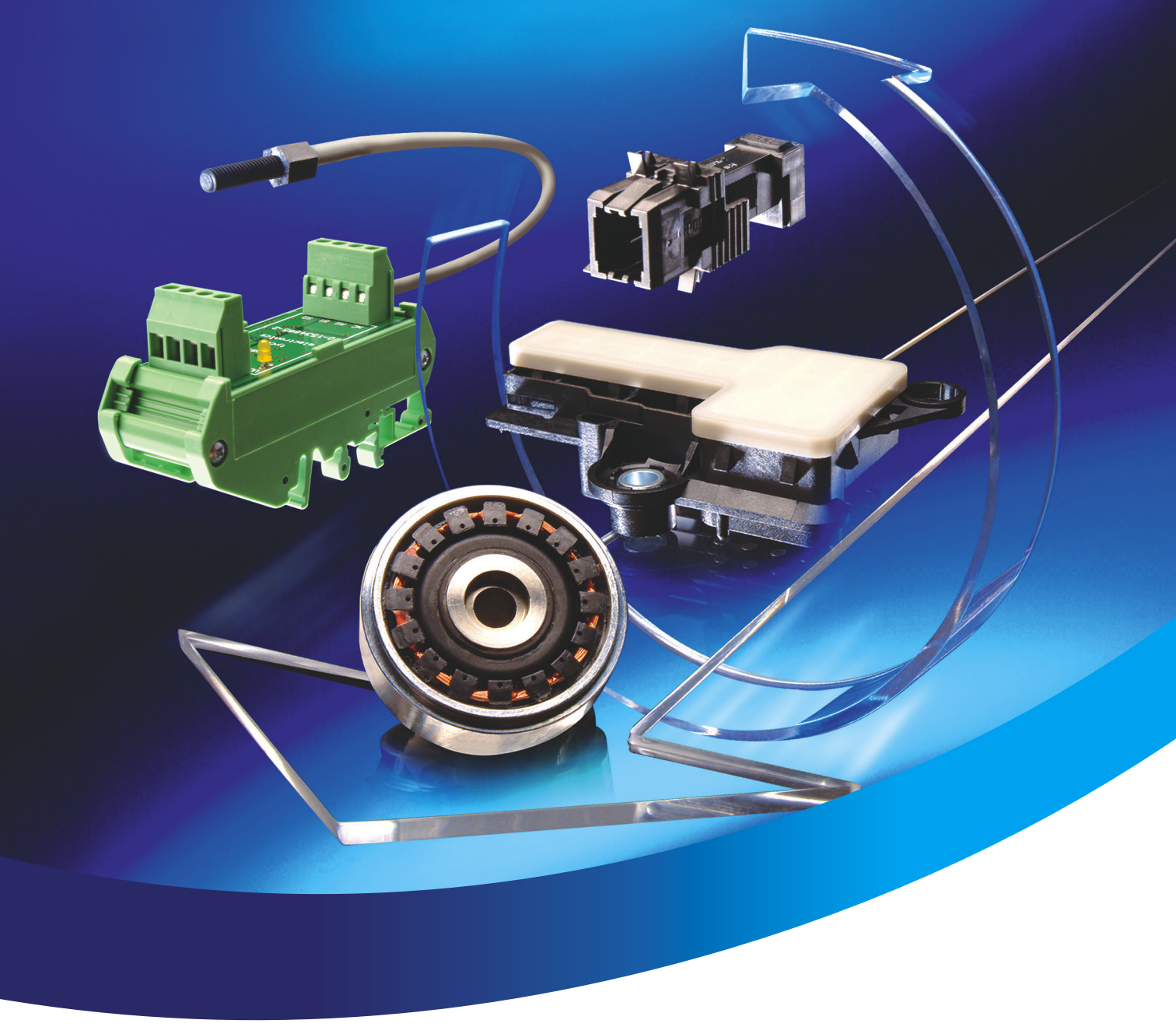


Figure 1 Open-Silicon has added or modified a significant number of stages (shaded) to its design flow to ensure manufacturability at the 90-nm process.



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thought his responsibility was to achieve timing closure, suddenly becomes responsible for a range of physical-design and process variables that are beyond his experience.

This scenario is frighteningly close to reality for the early-adopter design teams—the FPGA, memory, and CPU vendors—that are the pioneers on a process node. The responsibility for all these variables does indeed fall on the design team. To succeed, these teams form intimate relationships with their process providers, whether they are internal fabs or foundries. They also build cell-design, modeling, and process-engineering groups of their own to use the data that the fab-process engineers share with them.

However, this situation is untenable for ordinary cell-based-design teams and unthinkable for ASIC-design teams. That level of process knowledge would be impossibly expensive, even if, under some scenario, a giant foundry would share its basic data with an ordinary fabless customer. The industry is employing a number of tactics to breach this impasse. The earliest and simplest came into play at the 130-nm process and persisted into the early 90-nm designs. This era of the recommended design rule dictated that, by setting rules, the process engineers at the foundry could theoretically prevent design teams from putting anything into their physical design that would cause substantial variations in critical parameters. Then, by simply guardbanding the specs on the devices, and, at a higher level of abstraction, on the cell libraries the

DFM RAISES GLOBAL ISSUES

The global engineering community thinks that task management works without boundaries. With the possible exception of analog- and custom-design tasks, you can assign any block of a design to any available team anywhere in the world, and the results will be about the same. No interaction exists between culture and digital design.

But in the brave new world of DFM (design for manufacturability), the situation differs, say several experienced design managers. The reason hinges on one of the key differences between design at the 90-nm process and design at larger geometries. That difference is the role of judgment.

Until manufacturers arrived at the 90-nm node, design rules prohibited the features that would impact yield. You didn't put lines too close together for too long a distance, put corners of neighboring features opposite each other, and so on. If you tried to do one of these things, the DRC (design-rule-checking) tool would flag it, and somebody would fix it.

But at the 90-nm process, many of the rules–those that forbade features that were physically possible but likely to give low yields–became guidelines. "There are now so many recommendations that, if you followed them all, they would forbid you from doing your design," says Kazu Yamada, NEC's vice president and general manager for custom SOC (system-on-chip) products. On the other hand, if you ignore them all, you may never see double-digit yields from your product. And no magic tool exists that can tell you the impact on yield if you comply with one group of recommendations and skip the others in a block.

So, designing critical blocks at the 90-nm node and even more at the 65-nm node is a matter of judgment. And individuals approach such matters in a culturally conditioned way.

"Japanese people grow up thinking that risk is inherently evil," Yamada says. "Kids in the United States receive rewards for taking risks. And you see that in the behavior of engineers. Japanese design teams are good at absorbing a set of guidelines and identifying the points they need to pay attention to. US teams are more skilled at ignoring a set of risks and finding ways to quantify the results. You now need both cultural attitudes in a design, because if you paid strict attention to all of the yield issues at 65 nm, you would never complete a design."

Qualcomm Principal Engineer Riko Radojcic makes similar observations. "We have design centers in the United States, India, and other countries," he says. "We have some centers that are likely to question the design guidelines and others that may sometimes go too far in implementing them." Radojcic does not ascribe the whole difference to culture, however. He says that the boldest teams are often those that have an internal group of experts whose job is to convert the foundry's guidelines into a filter that designers apply to the design data. Those design centers that lack access to a resident group of experts tend to be less comfortable with the fuzziness of 65-nm design and to want hard and fast principles.

It may well be that an inherent uncertainty exists at the 65-nm node. You never know whether you have stayed close enough to the guidelines, but you always have to ignore some of them. This uncertainty illuminates individual differences in risk-taking behavior. Some designers accept the risks, whereas others, whether for cultural or personal reasons, assign that responsibility either to a tool or to an expert. This consideration may become significant in the management of global design resources.

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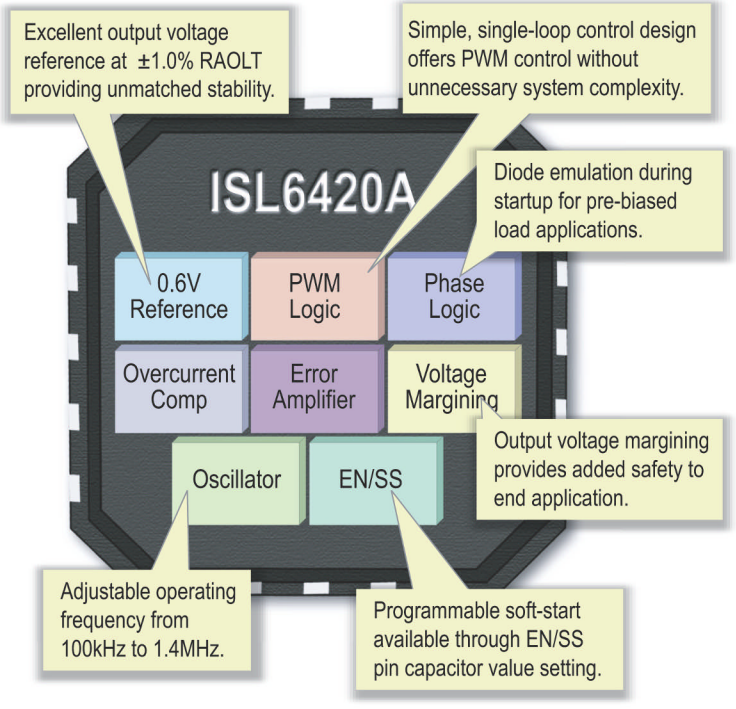

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foundries began to provide, the process folks could ensure that the chip designers—those who followed the rules, that is—would never get any negative surprises.

However, as they carried this approach into the 90-nm-process node, a negative surprise did occur. The foundry engineers kept finding new problems with each new design and creating new design rules to prevent them. Thus, for early 90-nm-process users—and not just the pioneers—the rules kept changing rapidly. Soon, one list became two lists: mandatory rules and recommended rules. Then, teams added guidelines. By now, design teams had three problems. First, there were so many rules that even checking for compliance was impractical. Second, complying with even a fair fraction of the rules negated most of the performance and density advantages of going to the 90-nm process in the first place. Third, under the rules, some important structures became simply impossible.

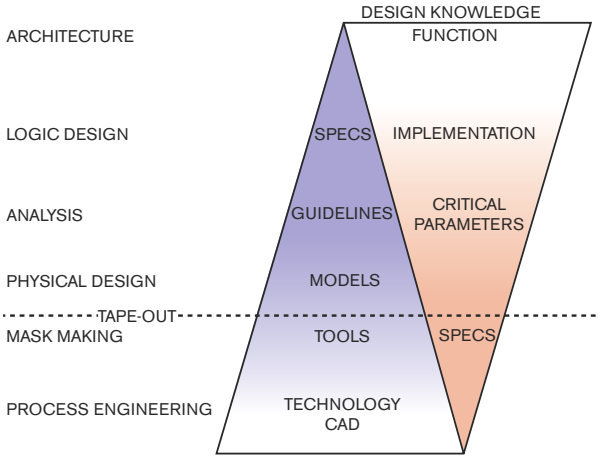

Figure 2 Process understanding is diffusing up into the chip-design team, growing more abstract as it moves up. Design understanding is diffusing down toward process engineering.

This situation will only get worse at the 65-nm node, according to Kazu Yamada, NEC Electronics America's vice president and general manager. "It's not just that we are checking many more rules," he says. "At 65 nm, adding rules doesn't solve the problem. If you take all the restrictions together, they forbid you to design your chip." So what comes after rules? An intermediate step must emerge between just telling a designer to follow the rules and making him understand the process implications of every node in the design. The simple answer is that models come after rules. In theory, you can identify all the sources of variation that create uncertainty in the timing on a net. You can then model these sources, either statistically or with physics-based models, and you can use the models to tell the designer just what the result of his choices will be. Ideally, the models would give designers data they could actually use: accurate parasitic values, delay figures, and currents.

Even better, you could incorporate the models into the placement-and-routing tools and even into the synthesis tools and floorplanners to create a fully process-aware design flow. The tools would handle all the issues that could lead to variability, so the designers could conduct their work just as they did at the 130-nm process, only with a few more tools and steps. Unfortunately, both of these scenarios are fictional. Part of the problem is the difficulty of modeling the process steps that contribute to the variability in the first place. Equipment vendors and process engineers employ PCM (process compact models), which are complex despite the term "compact." These models are too slow for chip-design teams or, in most cases, cell designers. Also, they include many inputs that are the sole concerns of the equipment and foundry industry. A model of CMP (chemical-mechanical polishing), for instance, might include inputs for pad composition, pad pressure versus time, back-plate structure, slurry formulation, location and time of the slurry's introduction to the wafer, rotational speed, temperature, and electric-field strength. And CMP is just one stage in the model.

"WE HAVE TO START OUT WITH THE PCMs AND ABSTRACT JUST WHAT THE DESIGNERS NEED."

Accordingly, EDA players are working—hesitantly, perhaps—with foundries and even more tentatively with equipment vendors to extract some data from the PCMs, turn them into simpler and more quickly executed models, and allow them to have inputs for things only under the control of the chip-design team. This effort is causing the growth of independent modeling within the EDA companies. "We have to start out with the PCMs and abstract just what the designers need," says Anantha Sethuraman, vice president for DFM at Synopsys. This abstraction yields a separate model of the process that must evolve with a rapidly changing situation. "The foundries work with us to update our abstracted models, and we pass the changes on to our customers," he says. "At 90 nm now, the processes around the industry are becoming similar, and they are becoming more stable."

David Thon, group director in the nanometer-analysis and verification group at Cadence, calls this process "adaptive abstraction." He describes a two-way flow of information across the interface between the design team and the foundry (**Figure 2**). As foundry information flows upstream to earlier parts of the chip-design process, abstract forms become more necessary. Although cell designers may need to know how to make painful trade-offs between speed and variability on a net, architects may need only abstract information about the structures and constraints that lead to a good yield. Conversely, mask makers who run the OPC (optical-proximity-correction) tools may need to have a reasonable understanding of the role a set of polygons plays in the electrical design. Process-integration engineers may need to have only an idea of performance and yield targets.

Currently, neither these models nor PCMs can provide accurate predictions of the electrical characteristics of a net or

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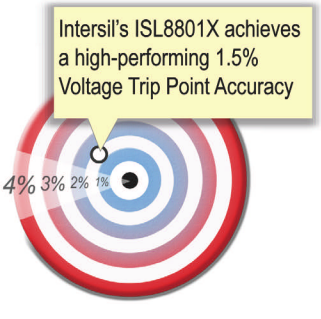
Dual Voltage Supervision		●			
Adjustable POR Timeout (C_{POR})	●			●	
Manual Reset Input ($\overline{MR}$)	●	●	●	●	●
Fixed Trip Point Voltage	●	●	●		
Adjustable Trip Point Voltage		●		●	●



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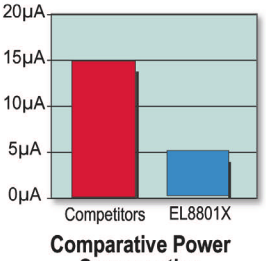

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accurate quantitative views of the impact that a design choice will have on die yield. "We can give designers some level of comfort, some idea of the impact of the changes they are making, and some idea of what definitely won't work," Sethuraman says.

Another limitation on the EDA industry's approach to the problem is that the industry has so far built abstract models of only those process steps whose variations engineers understand well. In reality, that limitation dictates two models: one for lithography—including, depending on whom you ask, more or less provision for modeling etch processes—and one for CMP. The industry then lumps anything else that occurs during wafer processing that can contribute to variability in electrical parameters under "variation." "There are 2000 or 3000 sources of variations in an advanced process," NEC's Yamada says. "It's impossible to put models of all of them into the EDA tools, and the EDA companies cannot do their own process models. All they can do is give us faster tools for dealing with the growing number of process corners, but we can't just keep adding more corners, either."

The consensus is that even the latest yield-aware tools still can't protect the design team from having to understand the details of the design process. There is some hope that at least these issues would affect only cell designers and custom-circuit designers. But manufacturers often can't fulfill that hope.

"We tried just guardbanding at 90 nm," Yamada says. "It resulted in chips that were either too big or too slow." NEC then incorporated deep awareness of variability issues into its cell libraries, so layout designers can now choose either conservatively designed, high-yield cells or aggressively designed, high-performance cells that exhibit greater variations. The physical-design team must assess its own risk and its understanding of the original design intent to make the selection.

This process draws a stark line between ASIC and COT (customer-owned-tooling) customers. "The ASIC customers just give us the design and expect us to deal with the DFM issues," Yamada says. "The COT customers, who typically are pushing the area/performance/power envelope, want to be intimately involved in the trade-offs between specs and yield at each critical spot in the design. They have to understand these issues in depth. The best of them have been through the experience before."

NEC's experience is that how far the need for process expertise penetrates into the design team depends on how hard the design pushes the envelope. If the point of using a 90-nm process is simply to make the die smaller and decrease dynamic power, a conventional team can turn over the RTL (register-transfer-level) logic with appropriate timing files and test cases to an ASIC vendor. If the point is to get a chip that is smaller, faster, and less power-hungry, chip designers must intuitively grasp how much risk they are buying in exchange for a more aggressive circuit design.

For example, Qualcomm uses an almost purely cell-based design flow for the 90-nm process, according to Radojcic. Many DFM guidelines existed for physical designers, but they handled DFM issues in the same manner as they performed DRC (design-rule checking)—that is, by running DFM-screening tools after layout. The company develops its own cell libraries, and its foundry runs internal inspection tools on the cell designs and suggests changes. But only the cell designers were privy to this information. "The foundry didn't require our design team to become lithography or CMP experts," Radojcic says.

The only big change at the 65-nm process was that the foundries gave their DFM-scoring tools to Qualcomm to run itself. Qualcomm used these tools primarily on individual cell designs, except in the case of full-custom blocks. The design teams did not mandate that a block had to achieve a particular score on the tools. In fact, designers often ran the tools in their spare time after tape-out. "We neither identified a yield issue using the tools, nor found the 'end of the world,' as some people have been predicting. We have had a good yield ramp on our 65-nm design," Radojcic says.

To deal with variations, the Qualcomm team stayed with traditional corner-case analysis. "In the brilliance of hindsight, we might have left the margins too big," Radojcic says. But that mistake may be an unavoidable cost of a design that depends not on process modeling or analytical tools that don't yet exist but on the skill and experience of master designers. "There is simply no way to relate design choices and DFM-driven modifications to changes in yield," he says. "In a way, the return on investment for all these tools, beyond what you get from the experience of your design team, is faith-based. Now, we are using our 65-nm design flow to evaluate changes to make DFM more formal at 45 nm." He says that there are two schools of thought on the subject: One says to go to SSTA and try to understand how to use it, and the other says to account for as many of the variations as

MORE DFM COVERAGE

The July issue of *EDN*'s sister publication, *Electronic Business*, explores a post-DFM (design-for-manufacturability) world in which the cost of chip design will be prohibitive. One theory posits that general-purpose chips will become the norm as high design and fab costs make custom chips uneconomical.

Whether or not you buy this scenario, there's little doubt that the relationship between design and manufacturing is changing dramatically. For more, go to www.eb-mag.com/dfm0706.

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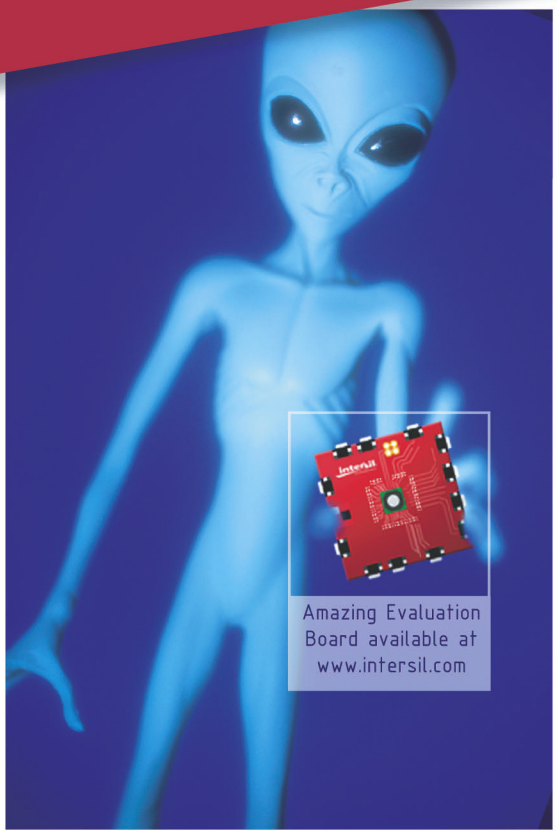

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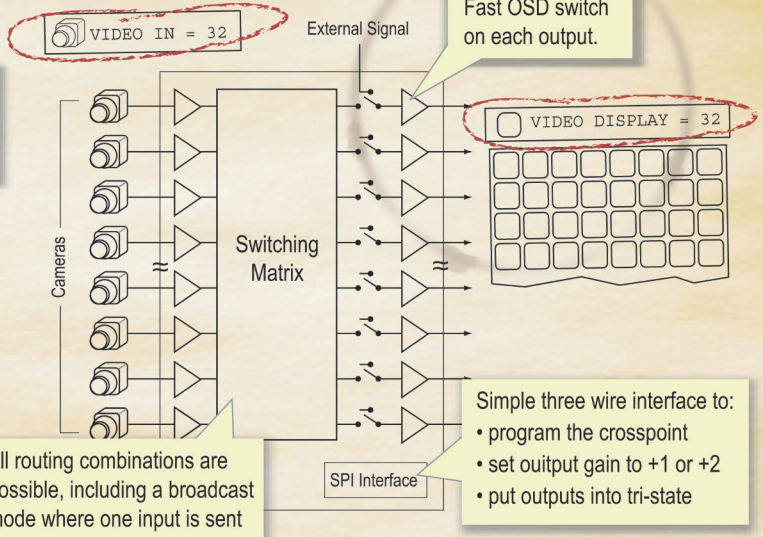

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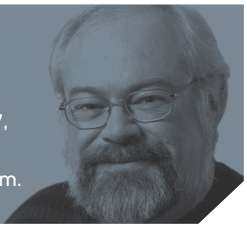
you can and accurately characterize them in the models.

When designers encounter a problematic structure, they must be able to do something about it. In this case, "something" does not mean tearing up the entire layer and doing a new layout based on handcrafted changes in the one problematic location. That approach would most likely lead only to the emergence of more problems elsewhere. So, EDA vendors such as Cadence have been working on incremental tools that will allow adjustment to a local portion of a layout; rescreening of the new layout for lithography, CMP, and DRC; and incremental modifications to the extraction files. Cadence believes that this approach requires a modification to the underlying structure of the design database, so that tools can identify objects in the neighborhood of a feature without traversing the entire database.

Ultimately, success depends upon the ability of master designers to take in data from a growing Tower of Babel of compliance checkers, rule checkers, and analysis tools and to base design decisions not on yield predictions, but on their own experience. TSMC (Taiwan Semiconductor Manufacturing Co), for its part, is trying to reduce the dissonance. For its 65-nm reference flow, the company has created a common data format for the eight DFM partners it has included in the flow. Using this format, it will put critical-area analysis, lithography-process checking, virtual-CMP modeling, and, in a later release, parametric modeling in the hands of chip designers. "We can't claim to estimate yields," says Edward Wan, TSMC's design-services senior director of product marketing. "But we can predict lithography and CMP hot spots in the design. We will base the sensitivity levels of the tools on our internal variation data, so that the tools can flag things that we know will not provide good yields. This approach will put fixing the problems within the range of back-end chip-design people."

You can reach Executive Editor Ron Wilson at 1-408-345-4427, ronald.wilson@reedbusiness.com.


But how much the designers have to know still comes down to how hard they are pushing the envelope. Bradley Howe, vice president of design engineering at early adopter and custom designer Altera, is more careful in his assessment of how well models and tools can shield designers. Howe believes that the company's experience may transfer to design teams that later join with more cell-based flows. "You probably can't just let the cell libraries deal with the problems, at least at 65 nm," he says. "I'm skeptical that you can encapsulate the knowledge of process variations into libraries or EDA tools without leaving big guardbands. That may be OK for some designs, but not for others. Granted we are a full-custom flow. But our experience has been that you can't limit the impact of DFM to some level of abstraction. It permeates all the way up to the architectural level. We found, for instance, that when we were developing the routing architecture for our 65-nm generation, we ended up knee-deep in transistor-dynamics issues. Everybody involved had to have some level of understanding."

This belief appears to be the fundamental change on the horizon for design teams at the 90- and 65-nm-process nodes. If you want to get what a process has to offer, you need individuals who can, based on their experience, their knowledge of the sources of variation, their control, and their impact on electrical characteristics, take calculated risks on a circuit-by-circuit basis (see **sidebar** "DFM raises global issues").

"My advice to a design team just starting out at 90 nm is: Don't wait. Bite it off now," says Howe. "Either hire the expertise you need or help your people develop it. You have to build this infrastructure inside your team, because, sooner or later, no tool or third party can make the problems go away." EDN

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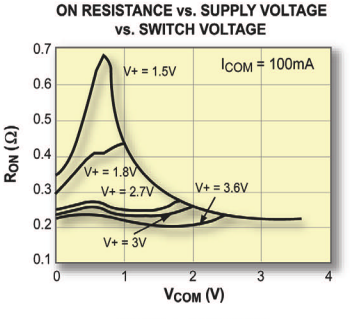
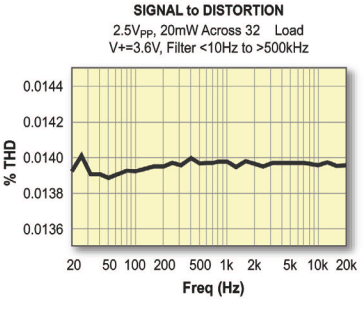
	ISL84715	SPST (NO)	0.26	0.04	4kV	1.6 to 3.6	SC70-5
	ISL84716	SPST (NC)	0.26	0.04	4kV	1.6 to 3.6	SC70-5
	ISL43L210	SPDT/2:1 Mux	0.44	0.06	6kV	1.1 to 4.5	SC70-6
	ISL43L110	SPST (NO)	0.26	0.04	4kV	1.1 to 4.5	SC70-5
	ISL43L111	SPST (NC)	0.26	0.04	4kV	1.1 to 4.5	SC70-5
Duals	ISL84762	2xSPDT/2:1 Mux	0.29	0.03	9kV	1.6 to 3.6	TDFN, MSOP
	ISL84684	2xSPDT/2:1 Mux	0.29	0.03	9kV	1.6 to 3.6	TDFN, MSOP
	ISL8484	2xSPDT/2:1 Mux	0.29	0.03	9kV	1.6 to 4.5	TDFN, MSOP
	ISL43L220	2xSPDT/2:1 Mux	0.23	0.03	9kV	1.1 to 4.5	TDFN
	ISL43L410	DPDT/Diff 2:1 Mux	0.29	0.03	9kV	1.1 to 4.5	TDFN, MSOP
	ISL43L120	SPST (NO)	0.17	0.008	8kV	1.6 to 3.6	TDFN, MSOP
	ISL43L121	SPST (NC)	0.17	0.008	8kV	1.6 to 3.6	TDFN, MSOP
	ISL43L122	SPST (Mix)	0.17	0.008	8kV	1.6 to 3.6	TDFN, MSOP
	ISL43L710	Diff SPST (NO)	0.17	0.008	8kV	1.6 to 3.6	TDFN, MSOP
	ISL43L711	Diff SPST (NC)	0.17	0.008	8kV	1.6 to 3.6	TDFN, MSOP
	ISL43L712	Diff SPST (Mix)	0.17	0.008	8kV	1.6 to 3.6	TDFN, MSOP
Quads	ISL83699	Dual DPDT/Diff 2:1 Mux	0.3	0.06	9/4kV	1.6 to 3.6	QFN, TSSOP
	ISL84780	Dual DPDT/Diff 2:1 Mux	0.45	0.07	4kV	1.6 to 3.6	TQFN, TSSOP
	ISL8499	Dual DPDT/Diff 2:1 Mux	0.3	0.06	9/4kV	1.6 to 4.5	QFN, TSSOP
	ISL43L420	Dual DPDT/Diff 2:1 Mux	0.3	0.06	9/4kV	1.1 to 4.5	QFN
Octals	ISL84781	8:1 Mux	0.41	0.056	4kV	1.6 to 3.6	TQFN, TSSOP
	ISL84782	Diff 4:1 Mux	0.5	0.056	4kV	1.6 to 3.6	TQFN, TSSOP
	ISL43L840	Dual 4:1 Mux	0.5	0.056	4kV	1.6 to 3.6	QFN, TSSOP
	ISL43L841	Diff: 4:1 Mux	0.5	0.056	4kV	1.6 to 4.5	TQFN, TSSOP

ISL84684 Typical Performance





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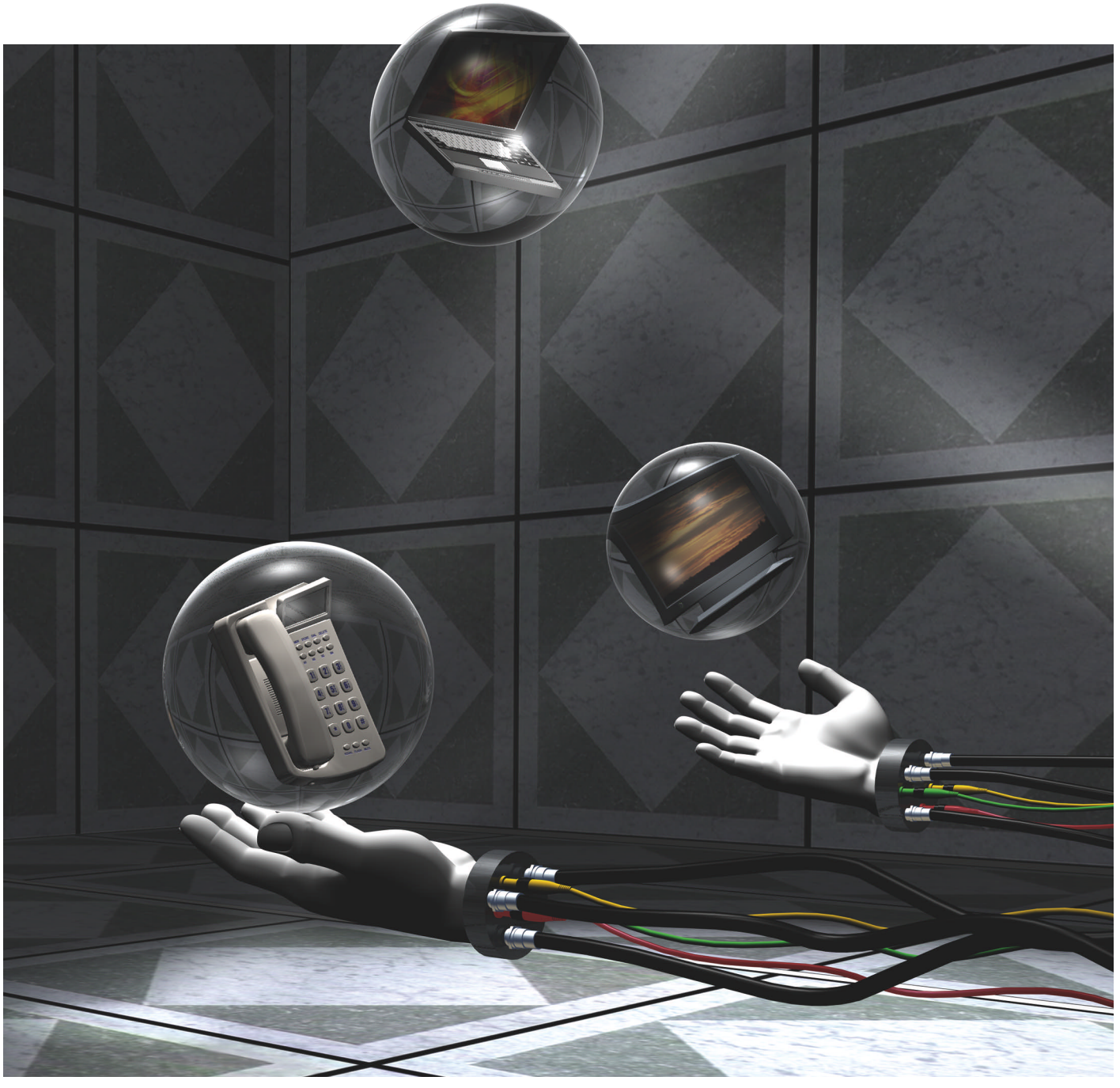

100-Mbps BROADBAND: HOW,

WHY, WHEN, AND WHERE?

A TRIPLE PLAY OF VOICE, VIDEO, AND DATA MOVES THE BANDWIDTH TARGET AS CONSUMERS ADOPT HDTV AND DVR TECHNOLOGIES AND DEMAND MORE CONTENT CHOICES.

BY MAURY WRIGHT • EDITOR IN CHIEF

Long the Holy Grail for telecom companies and MSOs (multiple-service operators), or cable companies, the triple play succinctly means serving consumers' voice, video, and data needs over a converged network. And without question, some telecom companies and MSOs are delivering today. But consumer desires are changing. Video has always been the most bandwidth-hungry part of the play, and that need for speed is skyrocketing. Consumers are increasingly enamored of DVRs that might record two or even more channels while yet another channel plays live. Combine DVR use with the escalating migration to HDTV quality, and the last mile is suddenly once again a huge obstacle just as it was for broadband data a decade ago. Purveyors of cable, DSL (digital-subscriber-line), and optical-network services all have plans to support the ramping bandwidth demand, but none of those plans is cheap or simple in deployment.

Next-generation broadband gates a number of services ranging from real-time and interactive TV to more compelling multiplayer gaming. And the impact and opportunity go far beyond the companies—the IC vendors, communication-equipment makers, set-top-box vendors, and service providers—that directly address the market. Next-generation broadband expands the market for home networking, entire new classes of consumer products, and content.

Consider the types of networks that now are or will soon be in deployment and the challenges the service provider face. Worldwide DSL is outpacing all types of broadband deployment. Optical is just getting started. In North America, cable may still be the market leader (see **sidebar** "DOCSIS moves ahead"). But Imran Hajimusa, director of marketing for communications-access ICs at Infineon, claims that three DSL lines are being deployed today for every cable line worldwide. DSL also faces perhaps the toughest challenge in the triple-play race.

THE DSL CHALLENGE

The challenge starts with the bandwidth requirement that telecom companies face with video-over-DSL services or IPTV (Internet Protocol television). In such a deployment, the telecom company sends only the video channels that the subscriber requests down the last-mile connection. Channel changes happen in the companies' remote terminal. IPTV software from companies such as Microsoft has progressed to the point that channel-change time is acceptable to consumers even though the channel request must go upstream to the telecom equipment.

But what can DSL data rates deliver? Starting in late 2004, many telecom companies moved to ADSL2+ (asymmetrical-digital-subscriber-line 2+) technology that boosted downstream data rates to 25 Mbps by doubling the transmission band to 2.2 MHz. Presumably, a telecom company can deliver one HDTV stream and two SDTV streams along with Internet service and VOIP (voice-over-Internet Protocol) phone service on an ADSL2+ line. But Infineon's Hajimusa claims that North American telecom companies have found such an offering insufficient. He claims that consumers are demanding six channels, two of which are HDTV. Hajimusa states, "Anything else is just rubbish. This is what the consumer is looking for."

Better video encoding can ease the video-bandwidth requirements. Originally, a typical MPEG-2-based HDTV stream needed close to 20 Mbps in bandwidth. Improved codecs get that number down to

AT A GLANCE

- DSL (digital-subscriber-line) deployments have passed cable on a worldwide basis, but DSL may face the toughest challenge of any option when it comes to video delivery.
- Consumers are demanding six channels, two of which must be of HDTV quality, in IPTV (Internet Protocol-television) applications. That demand translates to a minimum of 50-Mbps broadband services.
- PON (passive-optical-network) technology is taking off rapidly in Japan and to a lesser extent in North America. Aerially deploying the network on utility poles cuts cost and construction hassles.
- Hybrid-PON/DSL networks may offer the best bang for the buck in cities with copper-network installations.

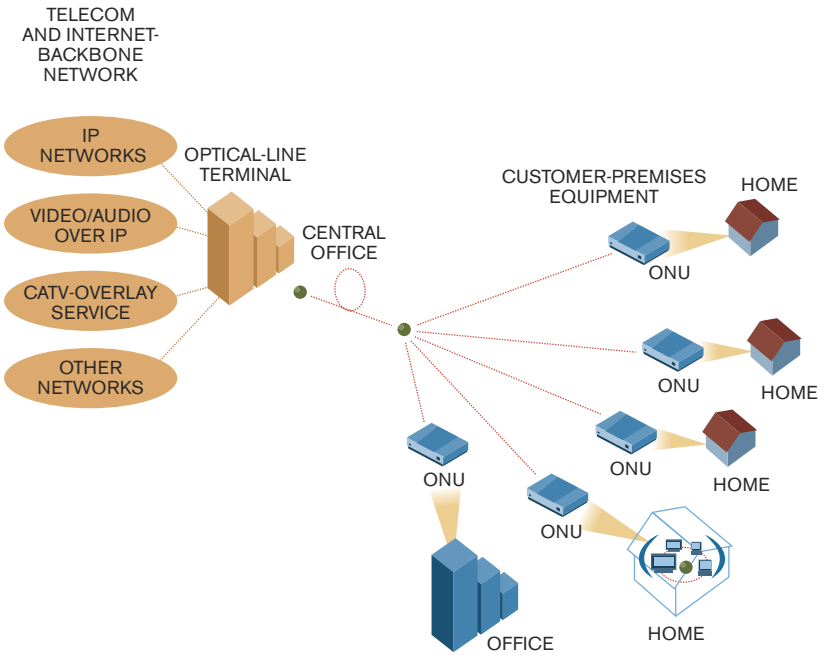

Figure 1 In a PON, an OLT (optical-line terminal) at the service provider connects to a fiber segment that is passively split, and the resultant fibers connect to either ONUs (optical-network units) or ONTs (optical-network terminals) at each subscriber premise.

approximately 12 Mbps. MPEG-4 helps even more. Cyrus Namazi, vice president of marketing at Conexant, claims, "Three HD streams require only 20 Mbps total with MPEG-4." Still, ADSL2+ can't meet Hajimusa's six-channel scenario.

The answer, according to DSL proponents, is VDSL2 (very-high-bit-rate DSL 2). The original VDSL standard offered higher data rates than ADSL, but QAM (quadrature-amplitude-modulation)-based VDSL was largely incompatible with DMT (discrete-multitone)-based ADSL. VDSL pioneer Ikanos had some limited success with VDSL, but telecom companies couldn't seamlessly migrate their customers to the faster technology. VDSL2 was completed a little more than a year ago and is both DMT-based and backward-compatible with ADSL2+.

Today, telecom companies can deploy VDSL2 chips in their remote terminals and support legacy ADSL clients, ADSL2/2+ clients, and VDSL2 clients. Hajimusa claims that Infineon can support 100-Mbps symmetrical VDSL2 service over distances as far as 3500 ft, using 30 MHz of bandwidth, or 50-Mbps symmetrical service over distances as far

TOO MANY PONs?

What would our industry be without competing standards, and why should we expect anything different in optical networking? Like skirmishes in the wireless-LAN- and ultrawideband-standards efforts, competing standards bodies have promulgated different versions of PON (passive-optical-network) technology, and vendors are deploying it in different scenarios around the world. Here's a quick guide to the PON flavor of alphabet soup.

The ITU-T (International Telecommunications Union-Telecommunications Standardization Sector) standard G.983 defines BPON (broadband PON). BPON is largely a follow-on to APON (asynchronous-transfer-mode PON), which still relies on ATM-transport protocols but at higher data rates. BPON offers asymmetrical service with 622-Mbps downstream transmission and 155-Mbps upstream transmission.

The IEEE-802.3ah standard defines EPON (Ethernet PON), or GE-PON (Gigabit Ethernet PON). As the name implies, EPON, or Ethernet in the first mile, carries native Ethernet traffic and offers symmetrical 1-Gbps service.

ITU-T standard G.984 defines GPON (Gigabit PON), which can support a variety of Layer 2 protocols, including ATM, TDM (time-division multiplexing), and Ethernet using the GEM (Generic Encapsulation Method) translation layer that the standard defines. GPON offers asymmetrical service with 2.5-Gbps downstream and 1.25-Gbps upstream transmission.

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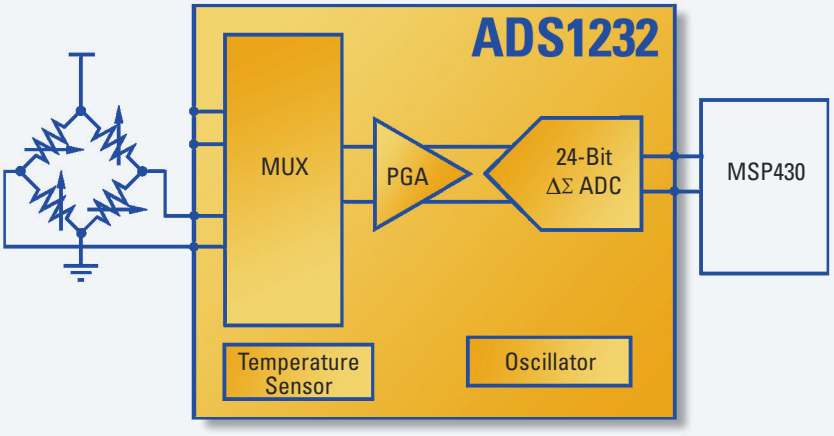

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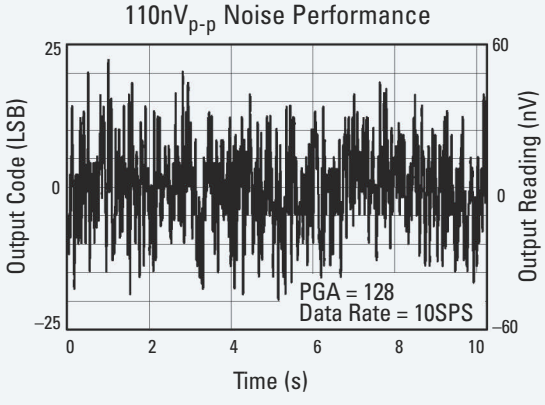

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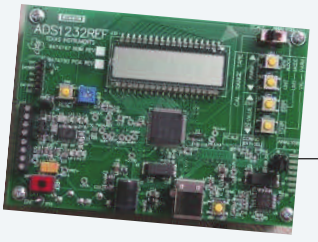

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as 5000 ft using 17 MHz of bandwidth. So telecom companies that deploy VDSL2+ on the service-provider side of the link can supply the six-channel IPTV example to customers with relatively short loops and still offer slower services for customers with longer local loops.

Today, Infineon, Conexant, Ikanos, and Broadcom are shipping VDSL2 ICs, and Texas Instruments has announced support through its Uni-DSL (Universal DSL) family. Still, debate is ongoing about how quickly VDSL2 support will proliferate. Hajimusa states, "There are some loops that will never get below 10,000 ft." Those loops wouldn't benefit from VDSL2 but would benefit from ADSL-2+. Supporting VDSL2 adds to the complexity of the silicon. "There is a premium to process 30 MHz of bandwidth," he says.

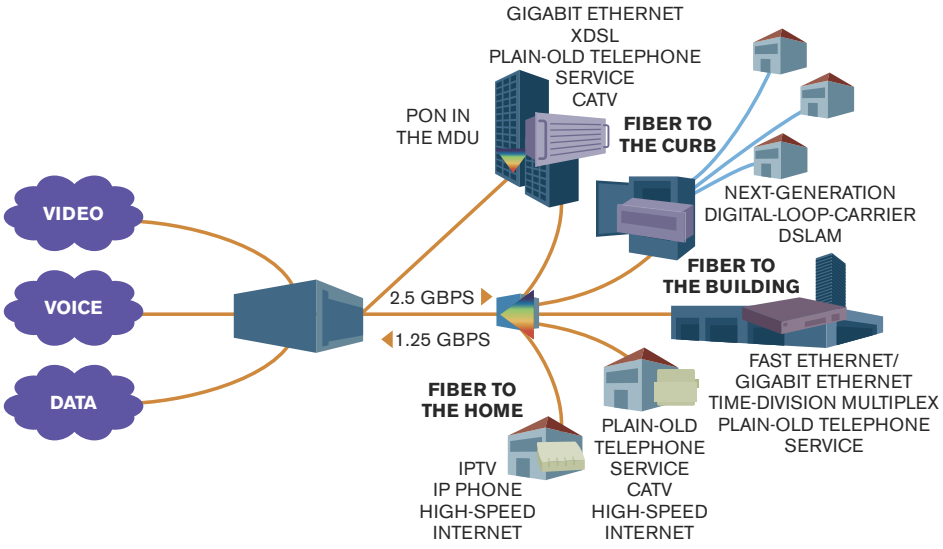

Figure 2 The variety of flavors of FTTx allows carriers to deploy fiber to individual homes or to deploy hybrid networks in which some flavor of DSL or another technology provides the final link to the subscriber.

Kurt Eckles, director of marketing for residential gateways at Texas Instruments, is more bullish on broad VDSL2 deployment. "The WAN interface is only 25% of our silicon costs, and a new process node will take care of that," he says. Eckles point is that power supplies, packaging, and other silicon dominate the cost of access cards in the remote terminal and in the CPE (customer-premises equipment). VDSL2 requires a relatively small premium to "future-proof" a network on the service-provider side, he says.

PONs DELIVER FTTH

But do technologies such as VDSL2 make sense with optical networks poised

MUNICIPALITIES ADOPT ACTIVE ETHERNET

Much of the optical-network deployment in North America today is in the form of the Active Ethernet switched network. The word "active" differentiates this type of network from PON (passive optical network). Unlike PON, in which a number of subscribers share the bandwidth of a single fiber segment, Active Ethernet is more like the typical office network in which each node connects to a central switch. And, whereas PON relies on passive splitters that provide the fiber drops to each subscriber, Active Ethernet requires a dedicated fiber to each subscriber.

Without question, Active Ethernet is superior to PON in the amount of bandwidth it dedicates to each user. PON proponents, however, believe that it would be cheaper to deploy the passive topology. PON requires only one set of optics on the service-provider side of the link, and its shared-media fiber plant is simpler. So, most large service providers worldwide are now pursuing some flavor of PON technology.

Active Ethernet proponents claim that the cost difference between the two has narrowed considerably as the price of optics has dropped. And Active Ethernet is winning business among new home communities that have FTTH (fiber-to-the-home) deployments, municipalities that deploy an FTTH network, and even some CLECs (competitive local-exchange carriers) that are deploying FTTH networks in competition with the major telecom companies.

In the case of small municipalities, the Active Ethernet deployment both serves the local residents and generates revenue. A typical municipality allows third parties to offer phone, video, and Internet service over the FTTH network. And the municipality gets a percentage of the revenue that the third parties generate. In such a scenario, Active Ethernet is more attractive to third-party service providers than PON would be because Active Ethernet provides dedicated and guaranteed bandwidth to each subscriber.

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to reach the home? Whether it's FTTH/C/P/N/B (fiber to the home/curb/premises/node/basement) or some other flavor of deployment, PONs (passive optical networks) are poised to push fiber nearer to the subscriber (see **sidebar** "Too many PONs?").

Generally, a PON in an FTTH deployment is more akin to a cable plant than a DSL plant (**Figure 1**). A typical segment of fiber serves 16 to 64 subscribers with passive splitters that create the fiber run to each subscriber. Downstream data rides one wavelength, and upstream data rides another. Even with the shared-media approach, a PON can provide a guarantee of 50-Mbps or faster services to a subscriber as long as the service provider manages the number of subscribers on each PON segment.

PON appears to be the choice of major service providers worldwide for optical deployment, although some smaller carriers and municipalities are installing Active Ethernet (see **sidebar** "Municipalities adopt Active Ethernet"). Considerable disagreement exists about which PON flavor will ultimately dominate. Carriers in North America and Europe prefer GPON (Gigabit PON) because it matches the carrier-class quality that the legacy carriers have always designed into their networks. Rich Moran, director of product management at NEC's Optical Network System Division, states, "GPON is well-suited to carriers because of its ability to tightly manage traffic and service." NEC is betting on GPON both in Moran's equipment division and in NEC Fiber Optek, which makes lasers and optical interfaces.

GPON is also the fastest flavor of PON, although speed to the subscriber depends on how many subscribers share an optical segment. EPON (Ethernet PON) proponents claim that EPON is cheaper and that the 1-Gbps rate allows EPON to use some components developed for 1-Gbps Ethernet. GPON advocates counter that, even though GPON is marginally more expensive, a GPON segment can serve double the subscribers of an EPON segment.

It would be nice if you could draw some conclusion by looking at early deployments of VDSL2 and PON, but it may be too early to judge those deployments. Moreover, hybrid PON/DSL networks enter the equation, as well. In North America, Verizon has the largest PON deployment; its FiOS (fiber-optic service) uses BPON (broadband-PON) technology to offer the triple play. BPON was a precursor to GPON, and Verizon will presumably migrate its network to GPON as chips and equipment become available. NEC's Moran believes that Verizon will make the GPON transition next year.

BroadLight supplies much of the BPON silicon that Verizon uses and is also the first company with broadly available GPON chips. "If it's just Internet, you can get away with BPON," says Dan Parsons, the company's director of marketing. Verizon now offers Internet and phone services over the broadband link on the FiOS deployment. The company offers the video services essentially through a cable-TV-like multicast service on an overlay network—a wavelength separate from the broadband service. Service providers in the future will have the

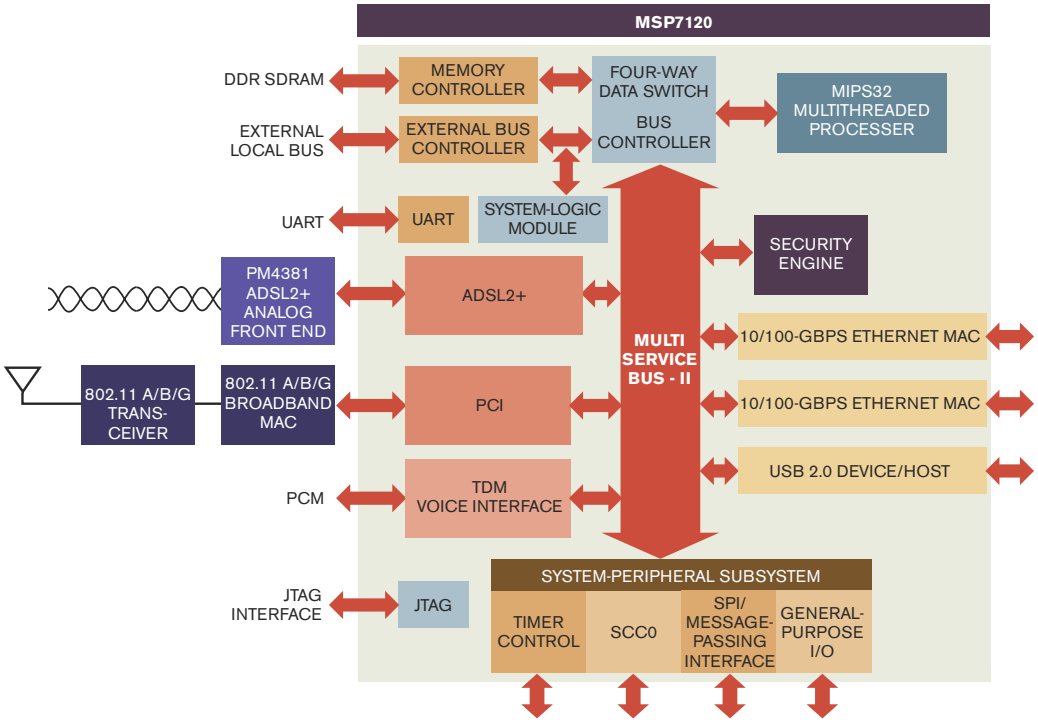

Figure 3 A family of chips for residential gateways, the PMC-Sierra MSP7100 gateway platform integrates ADSL and VOIP functions and can connect to home-network technologies, such as 802.11.

choice of offering video through a FiOS-like overlay, IPTV over the broadband link, or both. They could offer multicast video over an overlay and video-on-demand programs through IPTV.

The largest 1-Gbps PON deployment is the NTT (Nippon Telegraph & Telephone) EPON in Japan. Most experts predict that Japan, China, and Korea will drive PON deployment. In the case of NTT, the Japanese government has largely funded the EPON deployment that provides 100-Mbps services. The bandwidth may not be necessary today, but observers believe that it is important for Japan to lead the world in PON. Conexant's Namazi states, "In Japan, the claim that 'mine is faster than yours' carries a lot of weight. There is a lot of pride involved." Infineon's Hajimusa points out that some subscribers in Japan use 10- to 15-Mbps upstream rates for Internet gaming.

NTT based its deployment on ICs from PMC-Sierra through its acquisition of Passave. "The NTT new-PON-subscriber rate has passed DSL additions in Japan," says Babak Samimi, FTTH-product-line manager at PMC-Sierra. He claims that NTT is adding 400,000 to 500,000 PON subscribers per quarter. He also claims the number will reach 30 million subscribers by 2010 out of a worldwide PON deployment of 50 million to 60 million in 2010.

NTT aerially deployed most of its network on utility poles rather than burying it underground. The same situation is true of the Verizon BPON deployment. The combination of falling component prices and aerial deployment has decreased the cost of PON. Samimi claims that it can be as cheap as $600 to $700 to deploy service to a new subscriber. Others place the figure a bit north of $1000 but still far cheaper than the $6500 per subscriber it cost just a few years ago. However, many communities in North America don't allow overhead utilities, limiting the benefits of aerial deployment. Surprisingly, aerial optical plants are cheaper to maintain and more reliable that aerial copper plants.

Despite the success of PMC-Sierra in Japan, GPON proponents plan a major push across Asia. Presumably, NTT chose EPON because it was available and despite the fact that PMC-Sierra has been a sole source as an IC supplier. GPON proponents claim that the EPON standard leaves options, especially in areas such as security, that limit robust interoperability between chips from various vendors. Companies such as BroadLight believe that GPON interoperability will be key to ultimately winning a portion of the Japanese market, as well as in regions such as China.

Samimi counters that NTT added security provisions that make its EPON suitable for interoperability and that China can do the same thing. Recently, China held an EPON-interoperability test. Conexant is playing in both the GPON and EPON markets and participated in the Chinese tests. Conexant's Namazi states, "We have successfully interoperated with a number of companies in the EPON space."

Texas Instruments has yet to announce a PON play but is closely watching the market. TI's Eckles believes that China will focus on low cost and will ultimately choose a technology in which multiple vendors will compete and drive down component prices.

HYBRID-PON/DSL NETWORKS

Meanwhile, across the globe, hybrid networks will compete with PON FTTH deployments (**Figure 2**). For example, an FTTB or FTTN deployment might connect to the basement of an MDU (multiple-dwelling unit), such as a high-rise apartment building. Inside the building, VDSL2 might provide the link to subscribers over existing copper wires. Similar FTTN developments will serve individual homes. For example, Deutsche Telekom is using such an approach with VDSL2 to roll out a triple-play network in 10 major German cities. AT&T in North America is taking a similar approach. It could be that companies are deploying VDSL2 more in such hybrid networks than in pure-copper networks.

The hybrid-deployment concept eliminates the concept of a video-overlay network, such as the one that Verizon is using in its pure-optical BPON. If VDSL2 bridges the final link to the subscriber, then IPTV is the only option for video services.

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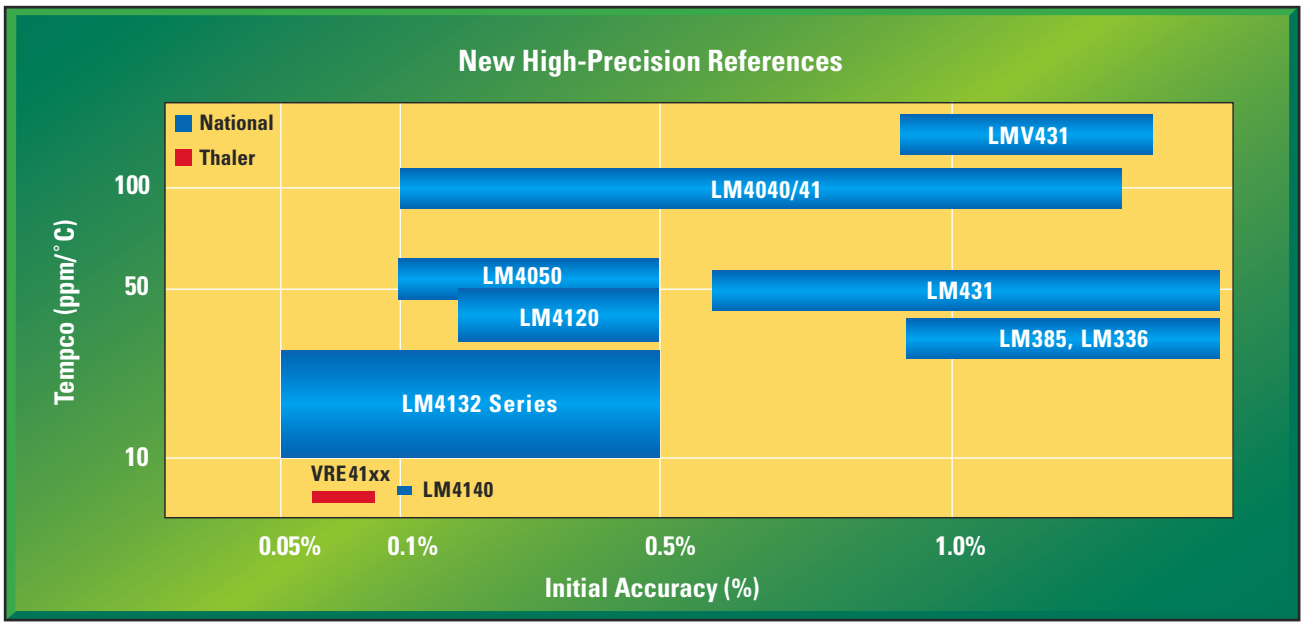

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A move of gear inside the home is another deployment trend to watch. As TI's Eckles points out, "The telco network has traditionally ended with the line pair. The telcos now want to move the demarcation point to CPE in the house. The cable industry always had that philosophy with the way they developed DOCSIS [Data Over Cable Service Interface Specification]." Conexant's Namazi agrees. "The service providers have wanted to sell the consumer more, but they have been afraid of the support issues," he says.

Both Eckles and Namazi are referring to the telecom companies' plan to move to a residential gateway. Both see the service providers providing consumers with a box that integrates 802.11 wireless-LAN technology or other home-networking technology for video distribution, VOIP telephony, and other services. The service provider might charge the consumer a premium for such CPE, but, realistically, the avenue to more services will generate revenue.

Still, such a plan opens the service provider to the support risk. But Namazi claims that implementing a gateway on an SOC (system on chip) would mitigate some of the support risks. "A gateway

DOCSIS MOVES AHEAD

At first glance, you might think the cable MSOs (multiple-service operators) have solved the triple-play issue of voice, video, and data and can count their money. In North America, where cable still dominates, the major players are offering the triple play, including HDTV and DVRs. But the MSOs will have their own set of problems as they continue to add intelligence to their network, push intelligence deeper into the network, and offer more HDTV content. For example, CableLabs is promulgating new DOCSIS (Data Over Cable Service Interface Specification) 2.0 and 3.0 standards.

The MSO industry has widely deployed DOCSIS 1.1 cable modems that added quality-of-service features to earlier products. The next move is under way to DOCSIS 2.0 and adds support for faster upstream data rates for applications such as Internet gaming. DOCSIS 3.0, meanwhile, will add channel bonding, thereby providing MSOs flexibility in even further increasing both upstream and downstream rates.

Among the biggest trends in cable-modem design, EMTAs (embedded multimedia-terminal adapters) add an application processor and VOIP (voice-over-Internet Protocol) support to the traditional cable-modem function, thereby supporting voice calls in a standard manner. Broadcom and Texas Instruments are leaders in the cable-modem market, although TI claims to be pulling ahead in EMTA deployments, and MSOs that want to offer voice services are also targeting such deployments.

Kurt Eckles, TI's director of marketing for residential gateways, believes that growth in the cable side of broadband will come as DOCSIS pervades everything on the network. "Demand for a DOCSIS function in all set-top boxes will drive cable growth," he says. Eckles also believes the DSG (DOCSIS-set-top-gateway) initiative will be key for next-generation conditional access.

The big obstacle ahead, however, is how to handle more content–specifically, more HDTV content. As the telecom companies move to IPTV (Internet Protocol television), so could the MSOs. But making such a move would render the DOCSIS CableCards obsolete–at least in terms of receiving the IPTV channels. Consumers can add CableCard modules to TVs or even Media PCs to integrate digital-TV tuning over cable networks. Converting analog channels is another way that the MSOs could add digital channels. But a move to IPTV or a reduction in analog channels will surely anger some segment of the subscriber base.

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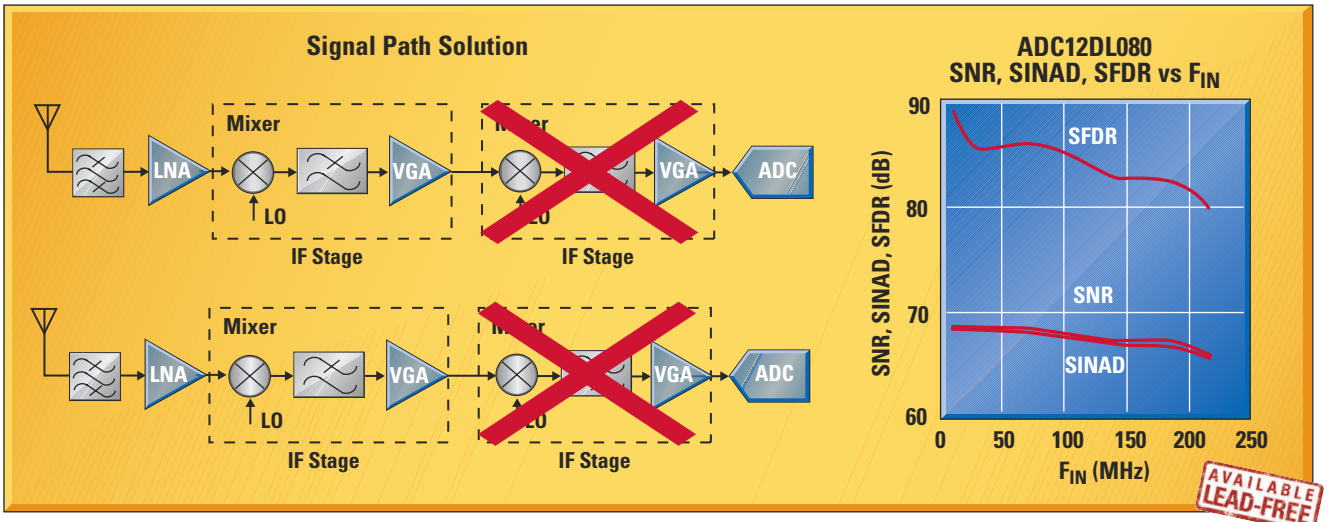

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with tightly integrated features is the only way you can get acceptable quality of service," he says. A networking-literate consumer can now cobble together home LANs with VOIP phone service. Namazi's point is that vendors will basically guarantee that the integrated functions in a residential-gateway chip will work as consumers expect.

As you might expect, CPE-chip vendors are moving toward the gateway trend. Texas Instruments has long offered such gateway reference designs. Recently, Broadcom, Conexant, and PMC-Sierra joined the market. Conexant introduced the CX9461x IC with an ADSL2+ modem, integrated 802.11a/b/g support, and VOIP features. Meanwhile, PMC-Sierra's MSP7100 gateway platform includes models for ADSL2+, VDSL2, and PON CPE, although the chips lack integrated 802.11 support (**Figure 3**). Similarly, Broadcom offers the BCM6358 with no integrated 802.11 support but pairs it with a new Intensi-fi 802.11 chip that the company claims is 802.11n-draft-compatible.

PATIENCE

In any event, the players in the PON and even the VDSL2 markets will need patience to realize a return on their R&D dollars. GPON hopeful AMCC (Applied Micro Circuits Corp) is working on a PowerPC-based MAC (media-access-controller) chip and now offers a PHY (physical)-layer chip. Neal Neslusan, director of marketing for the company's Transport Group, states, "From the time we kick off a program until we get a production part, it's 18 months to three years. Then, you get design wins, and that takes a couple of more years." Neslusan doesn't mention the need to guess right on the technology. And he isn't the only one looking at protracted deployment scenarios. For example, Conexant's Namazi states, "China is modifying the spec for encryption. That leads me to believe that massive deployment is a little way off." EDN

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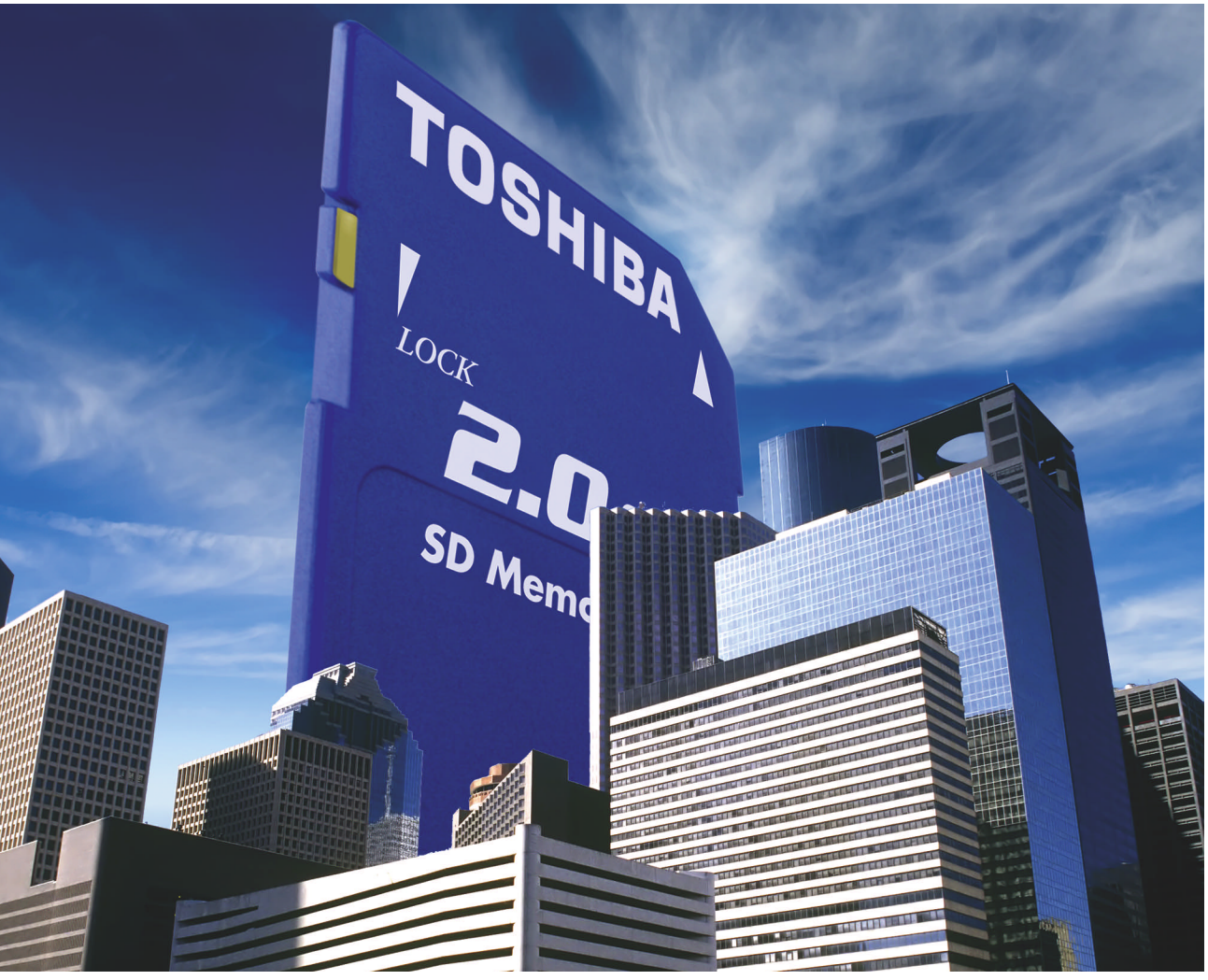

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Isolating USB

WITH ISOLATION, THE USB FITS A WHOLE NEW CROP OF APPLICATIONS.

Although designers rely on the industry-standard USB (Universal Serial Bus) port to interface computers with hundreds of custom peripherals, isolation issues restrict its use in many applications. Isolation improves common-mode voltage, enhances noise rejection, and permits two circuits to operate at different voltage levels. Two obvious areas that require isolation are the medical field, in which PC-based instruments attach to patients, and the industrial arena, in which large supply-rail offsets can occur. Thanks to its simple, four-wire structure, USB may appear to be a natural interface for electrically isolating a device that connects to a PC.

USB enjoys extensive industry support and has become the standard way to connect peripherals to PCs. The interface operates at the low speed of 1.5 Mbps, full speed of 12 Mbps, and high speed of 480 Mbps. This article deals with optical isolation for a full-speed USB connection. A 12-Mbps device operates with enough bandwidth for useful data transfers and employs a data rate that inexpensive optocouplers can manage. The USB connector contains four wires. Two, bus voltage and ground, supply power, and two, D+ and D−, move the USB data. The bus-voltage wire provides 5V at as much as 500 mA of current-sourcing ability. The bidirectional D+ and D− signals operate at a 12-Mbps signal rate, or 83 nsec per bit cell. The D+ and D− signaling voltage is 3.3V.

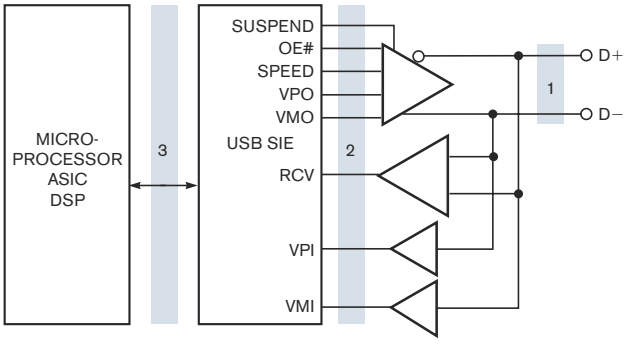

Figure 1 You can isolate a USB peripheral using the USB itself, the transceiver interface, or the application interface. Most current designs integrate the serial-interface engine and the transceiver, making the transceiver interface inaccessible.

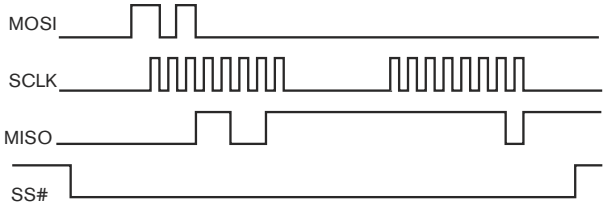

Figure 2 This serial-peripheral-interface example operates in mode (0,0). The same interface can operate in mode (1,1) if you make the SCLK signal active-low and the quiescent state is high. You can easily optically isolate these low-frequency signals.

Manufacturers build USB peripherals using a USB transceiver that connects to the D+ and D− lines and either drives or receives under control of an OE (output-enable) control pin (**Figure 1**). The middle portion, a USB SIE (serial-interface engine), handles translation of the bus signals that the transceiver sends and receives into data bytes and USB signals, respectively, for the application that implements the USB peripheral. The application circuitry might be a microprocessor, an ASIC, or a DSP.

ISOLATION SITES

You could incorporate optical couplers to electrically isolate a USB device from the host computer at the USB itself, the transceiver interface, or the application interface. Optical isolation on the USB wires is impractical, however, because the signaling rate is 12 MHz, which is too high for cost-effective isolators. Also, you must carefully match the D+ and D− signals for propagation delay and skew—a difficult prospect when using optical isolators. In addition, the USB is bidirectional, whereas isolators are unidirectional, complicating the situation. Furthermore, in a peripheral with an integrated transceiver, the OE signal, which indicates direction, is inaccessible.

A USB peripheral that uses an external transceiver exposes the transceiver interface, so you could consider these unidirectional signals for optical isolation. However, this site has the same problem as that for the bus wires: Its data rate is too high. It also has more 12-MHz signals to isolate. Signals VPO (single-ended output for D+), VPI (single-ended input for D+), VMO (single-ended output for D−), VMI (single-ended input for D−), and RCV (single-ended receiver output) all operate at 12 MHz, and you would need to carefully match them for delay and skew. Furthermore, this interface is rarely accessible in modern USB designs that incorporate the SIE and transceiver in the same chip.

The application interface is the most promising place to per-

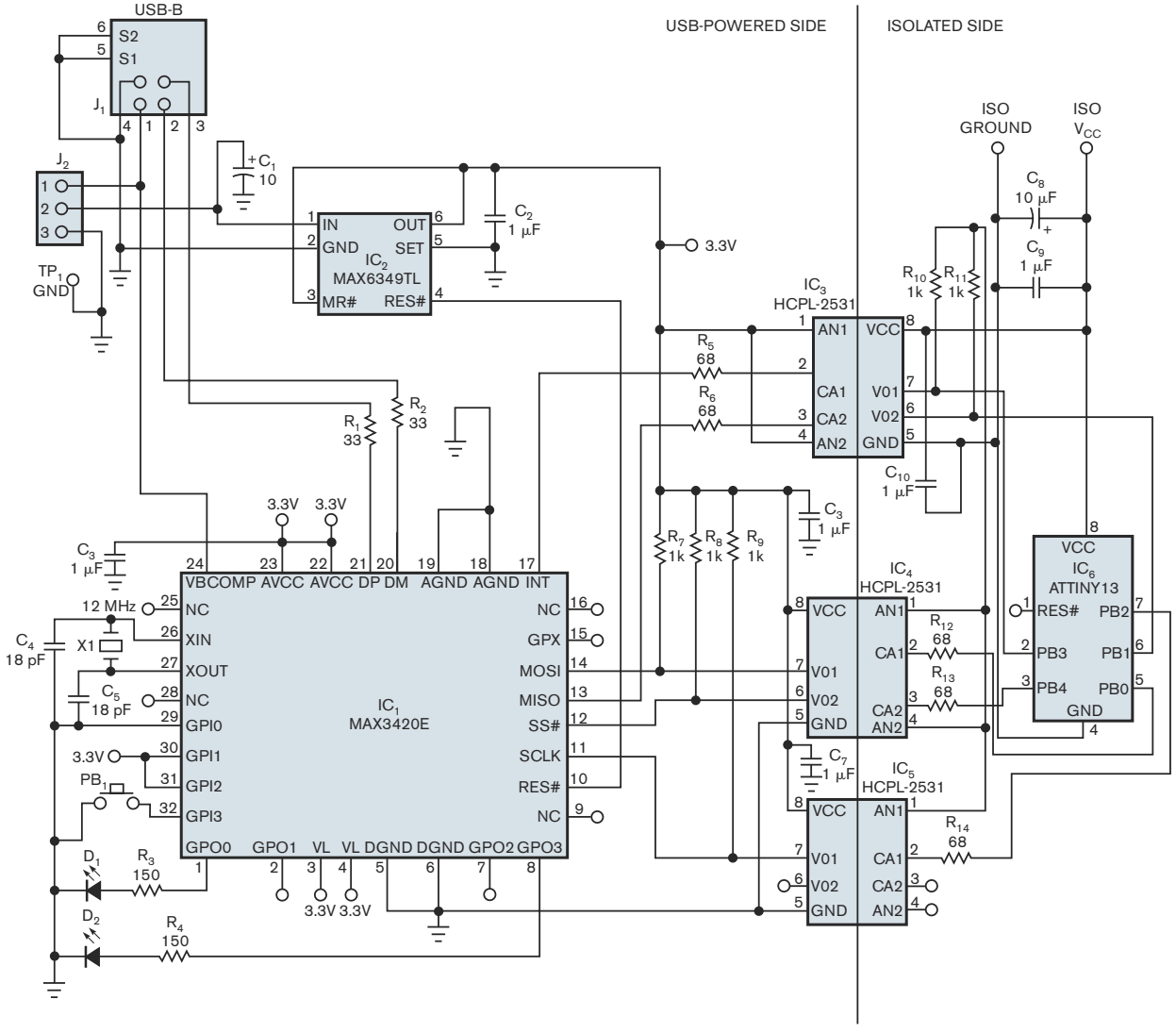

Figure 3 The USB powers the left side of this isolated-USB design, and the right side uses an isolated power supply. Providing the isolation at the SPI makes the design simple and independent of stringent USB timing.

form isolation, because the signals can operate more slowly than the USB data rate and you can build the interface so that it uses only unidirectional signals. An ideal interface would use a few unidirectional signals that operate at a data rate much lower than the USB's 12-MHz signaling rate. The SPI (serial-peripheral interface), which Motorola (www.motorola.com) originally defined and which is now widely available in many types of semiconductors, meets these requirements. This popular interface features simplicity and high performance.

TABLE 1 SPI SIGNALS

SPI signal	Description	Comments
SS#	Slave select	Selects the chip for data transmission, which the master supplies
MOSI	Master out/slave in	Unidirectional data pin
MISO	Master in/slave out	Unidirectional data pin
SCLK	Serial clock	Serial clock, which the master supplies

With the SPI, a master/slave system, the master initiates and conducts transactions to a single slave. The master provides the SS# (slave-select) signal and the SCLK (serial clock) to synchronize data transfers (**Table 1**). The SPI has four clocking modes, reflecting two CPOL (clock-polarity) mode signals and two CPHA (clock-phase) signals. An SPI data transfer between a microprocessor and an SPI-slave device commonly uses SPI mode (0,0) (**Figure 2**). In mode (0,0), the clock is low in its inactive state, and the SPI master makes the MOSI (master-out/slave-in) data available before the first SCLK positive edge.

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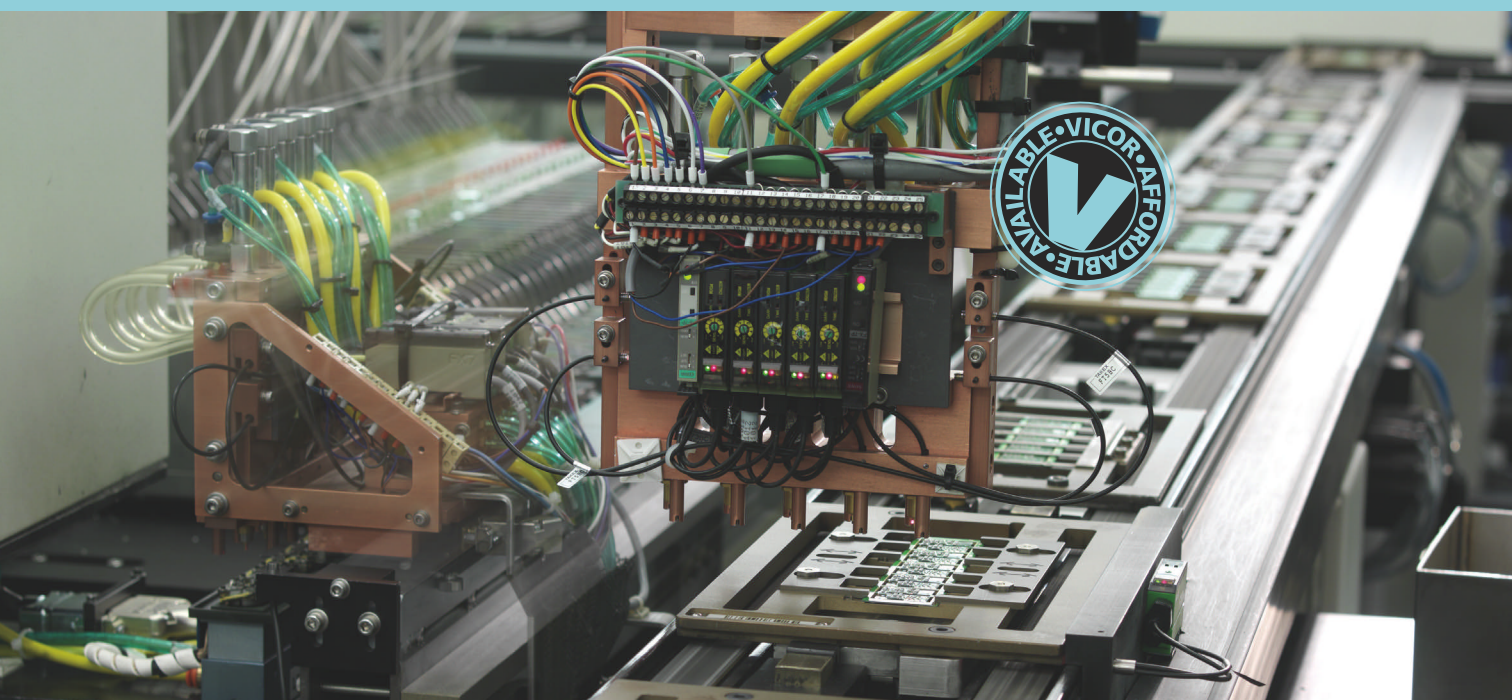

LISTING 1 MAX3420E CODE

```
; ------------------------------------------------------------------
; Read a MAX3420E register. Uses MAX_Reg(preserved), Updates MAX_Dat.
; ------------------------------------------------------------------
rreg:
      clT
rr2:  mov         dat,MAX_Reg ; 000rrrrr
      lsl         dat         ; 00rrrrr0
      lsl         dat         ; 0rrrrr00 (R)
      lsl         dat         ; rrrrr000  (write bit is clear--bl)
      bld         dat,0       ; rrrrr00T  (T=ACKSTAT bit)
      rcall       send_byte
;
; Now read the MISO data
;
      SCK_LO
r4:   SCK_HI                  ; ready the next input bit
      sec                     ; speculatively set CY
      sbis        PINB,MISO   ; skip if set
      clc
      SCK_LO
      rol         MAX_Dat     ; shift CY into the data byte
      dec         bitcount
      brne        r4
      SS_HI                   ; all done
      ret
;
```

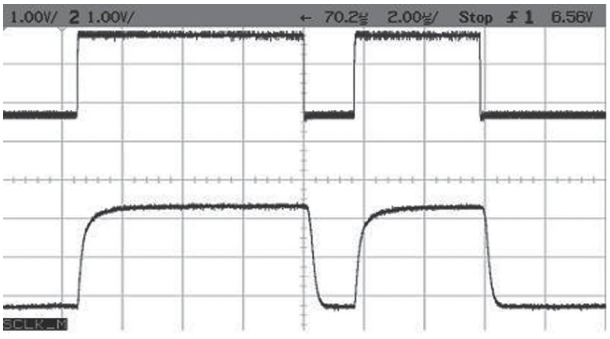

Figure 4 The SPI SCLK signal appears on both sides of the isolated interface. The top trace indicates the isolated supply at Ground 2 of 5V and V_{CC} of 8V.

For both master and slave devices, SPI data changes on the SCLK falling edge and is sampled on the SCLK rising edge. SPI is easy to implement on any microprocessor, even one that contains no hardware-SPI unit. All it takes is four general-purpose-I/O pins to construct the signals and two subroutines to read and write bytes by directly toggling the I/O pins.

The data rates of the SPI bus and the USB differ dramatically. The isolation approach becomes simple with the SPI signals, which you can tailor to run at any frequency to suit the characteristics of the optical isolators. The system reconciles the wide difference in data rates between the SPI bus that operates the USB controller and the USB signaling rate using USB's "self-throttling" feature with built-in flow control. It uses an NAK (negative-acknowledge) handshake, whereby a peripheral tells the host asking for data that it is not ready with data, and the host should try again later (see **sidebar** "USB-flow control"). Thus, a designer can fine-tune the SPI data rate to suit optocoupler choices for practical and cost-effective designs.

ISOLATED-USB-DESIGN EXAMPLE

Figure 3 shows a circuit based on an inexpensive microprocessor, the Atmel AtTiny13, IC_6; HCPL-2531 optocouplers

USB-FLOW CONTROL

Figure A shows the USB (Universal Serial Bus)-flow-control mechanism in action. Starting with Packet 362, the host issues a "get-descriptor-configuration" request. The 09 in the second-to-last byte of Packet 363 indicates that the host wants 9 bytes of data from the peripheral. The peripheral acknowledges receipt of the request in Packet 364 and then gets busy decoding the request and loading the requested data into its endpoint 0 data FIFO.

A slow peripheral takes some time to answer this request, and the relatively slow SPI (serial-peripheral-interface) bus increases the response time. After Packet 364–988.667 µsec later–the host starts asking for the requested data in Packet 366. The peripheral doesn't yet have the data, so the USB hardware automatically responds with the NAK (negative-acknowledge) handshake, indicating "I'm busy; try again later." The host tries again in Packet 368 and gets the same NAK answer from the peripheral.

This process continues until Packet 419, when the peripheral at last has the requested data and arms its endpoint 0 for the data transfer. Now, instead of NAK, it responds with the 9-byte data packet in Packet 420, which the host acknowledges in Packet 421. The NAK pairs (dotted rectangle in Figure A) can occur any number of times, which means there is no lower limit on the rate at which the SPI can operate.

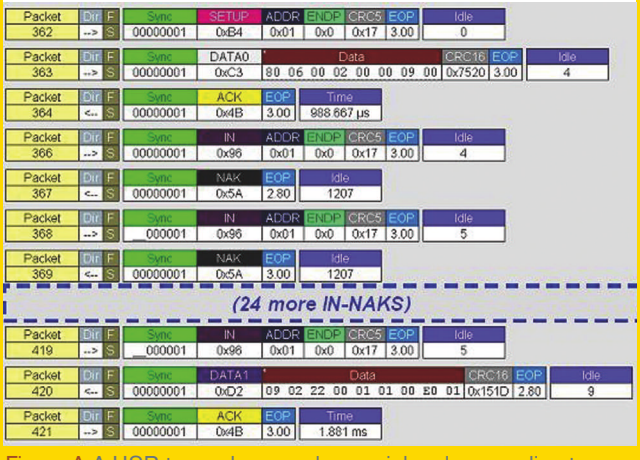

Figure A A USB trace shows a slow peripheral responding to a host's request for data. The host requests the data in packets 362 through 364. The peripheral is ready with the data in Packet 420. The intervening NAK packets demonstrate USB-flow control. The peripheral responds with NAKs until it is ready with data.

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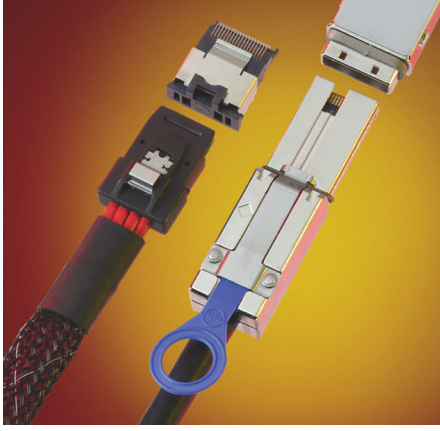

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IC_3, IC_4, and IC_5; and the MAX3420E, IC_1, a USB peripheral controller with an SPI to its register set. Even though IC_6 contains no hardware-SPI unit, "bit-banging" some general-purpose-I/O pins easily manages the SPI. IC_1 provides four general-purpose input pins and four general-purpose output pins to replace and add to the pins the microprocessor uses to implement the SPI. This design uses two output pins to drive LED indicators D_1 and D_2 and one input pin to connect the pushbutton switch S_1. Because IC_1 contains I/O pins of its own that SPI controls, they are inherently isolated from IC_6 and require no individual isolation.

Scope traces of the SCLK signal on both sides of the isolated interface demonstrate the optocoupler performance (**Figure 4**). The optocouplers have a throughput delay of approximately 0.5 µsec with the resistor values for this design. The short SCLK pulse in the center is the result of a portion of IC_6's code that drives the SCLK I/O pin (**Listing 1**). Just before the "r4" label, the SCLK signal is driven low and then immediately high again. Assembler macros SCK_LO and SCK_HI ease the assignment of I/O pins for pc-board layouts without changing the code. By inserting a few NOP (no-operation) instructions between these two statements, you can lengthen the narrow pulse in **Figure 4**, opening the possibility for using lower cost optocouplers. This example shows the flexibility that the SPI offers for optically isolated systems.

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Electrically isolating the USB has been a challenge due to the high-speed, bidirectional nature and stringent matching requirements of the USB-data signals. The situation becomes simpler if you isolate the interface between the USB controller and the application processor, because this interface can run at any rate. The lower signaling rate suits USB for low-cost optocoupler systems. As with any isolation design, the fewer lines that require isolation, the more cost savings you accrue. The SPI is an ideal candidate for isolation because it uses only four low-speed, unidirectional signals. EDN

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Lane Hauck works in San Diego, CA, as a senior scientist at Maxim Integrated Products (Sunnyvale, CA), where he has worked since 2002. He received a bachelor's degree in physics from the University of California—Los Angeles and a master's degree in computer science from California State University—Los Angeles. His personal interests include music and digital photography.

Reducing Switcher EMI with Spread Spectrum Technology

High Performance Analog Solutions from Linear Technology

Offering a significant space and efficiency advantage over linear regulators, switching regulators continue to expand into an increasing number of applications. One trade-off, however, is the potential for electromagnetic interference (EMI). Switching regulator EMI, a result of the internal switching current, is traditionally controlled and contained with a combination of grounding, shielding and filtering. In addition to these techniques, decreasing the peak switching current and altering the switching frequency can also reduce EMI. With this in mind, Linear Technology developed the LTC6902 and LTC6908 silicon oscillators specifically for the reduction of EMI by intelligently controlling the switching regulator clock.

Since their introduction, Linear Technology's silicon oscillators have proven their versatility across a wide range of clock applications. These solid-state devices generate precise square-wave signals without a crystal or ceramic resonator and without an external resistor-capacitor time constant. They have outstanding environmental characteristics such as inherent immunity to shock, vibration and acceleration, in addition to an operating temperature range from -40°C to 125°C. Output frequency range spans from 1kHz to 170MHz, start-up is consistently fast, power consumption is low and the footprint is as small as 2mm x 3mm. Since silicon oscillators are programmable, they can intelligently control a clock frequency with multiple phases. Specifically, they are ideal for multiphase synchronization and spread-spectrum frequency modulation (SSFM).

Why is EMI Important?

Tremendous growth in the use of portable electronics has increased the potential for EMI between devices. EMI can be a nuisance, as in the case of noise in a television or radio receiver. EMI can impair electronic device operation, such as avionic equipment, which is why airlines ban the use of portable electronics during take-off and landing periods. Underscoring the importance of this issue, government regulations have established EMI limits and test methods to ensure that products operate without experiencing interruptions and without interrupting other devices. Testing and tracking down EMI requires a lot of time and effort, so taking a proactive design approach to avoid last minute modifications and time-consuming retests is always a good idea.

Multiphase Synchronization

The current waveform in a switching regulator is irregular, producing EMI concentrated at the switching frequency. Instead of using a single switcher, multiple switchers synchronized out of phase will have a lower peak current and therefore lower EMI. This phase-synchronization is achieved by using a single clock with a phase shift placed between each regulator. This technique staggers the turn-on time of each switcher such that there is input current where previously there was a dead band. Figure 1 illustrates two switching regulators operated with a single 200kHz clock with the resulting peak input currents. Placing a 180° phase-shift on the 2nd regulator clock results in smaller current peaks at twice the

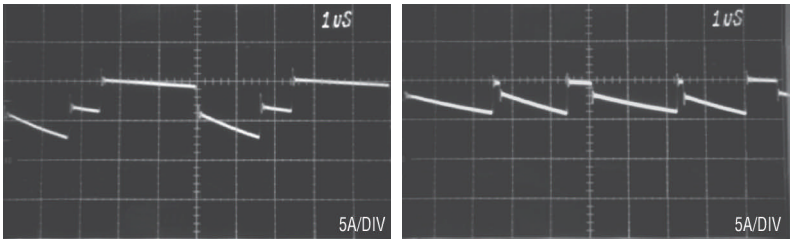

Figure 1. Supply Current for 2 Switching Regulators Operated without and with Phase-Synchronization

frequency (400kHz), and therefore smaller peak EMI. Since EMI is now at twice the frequency, it is further reduced since filtering is more effective at higher frequencies. Many dual and multiphase regulators take advantage of this technique by including built-in clock phase shifting. For example, Linear Technology's LTC3728, a dual 2-phase regulator, internally generates a 180° phase shift between the two regulator clocks.

A separate external clock with multiple phases is useful for synchronizing multiple dual or multiphase regulators, or when power requirements dictate the use of separate regulators. For these applications, Linear Technology's LTC6902 silicon oscillator provides 4 outputs, programmable for 2, 3 or 4 clock phases. Linear Technology's LTC6908 takes a simpler approach by providing 2 outputs available in 2 versions; the LTC6908-1 has two outputs with 180° phase-shift between them and the LTC6908-2 has two outputs with a 90° phase shift between them. The former is ideal for synchronizing 2 single switching regulators and the latter is ideal for synchronizing 2 dual, 2-phase switching regulators. For EMI improvement, however, phase-synchronization is only part of the story.

Additional Benefits of Multiphase Synchronization

In addition to improved EMI, using multiphase synchronization with parallel regulators has a net effect of canceling ripple currents on the input and output. This allows for a significant reduction in input and output capacitors. A multiphase solution has a smaller equivalent inductance and therefore, can provide a higher current slew rate. A multiphase solution also has less switching time delay for a load transient. As a result of the improved load transient response, the needed output capacitance is further reduced.

Spread Spectrum Frequency Modulation (SSFM)

The most dramatic improvement to EMI may be achieved by continuously varying the switcher's clock frequency. The technique, referred to as SSFM, improves EMI by not allowing emitted energy to stay in any receiver's band for a significant length of time. The effectiveness of SSFM with switching regulators depends upon the amount of frequency spreading, typically ±10%, and the modulation profile.

Various methods of frequency spreading are used for SSFM, such as modulating the clock frequency with a sine wave or a triangular wave. Most switchers exhibit ripple that varies with frequency; more ripple at lower switching frequencies and less at higher switching frequencies. As a result, a switcher's ripple will exhibit an amplitude modulation that follows the clock's modulating signal. If the clock's modulating signal is periodic, there will be a periodic ripple modulation and a distinct spectral component at the modulating frequency. Since the modulating frequency is much lower than the switcher's clock, it may be difficult to filter out. This could lead to system problems such as audible tones or visible display artifacts due to supply noise coupling or limited power supply rejection of the downstream circuitry.

To avoid this periodic ripple, Linear Technology's LTC6902 and LTC6908 silicon oscillators use a pseudorandom frequency modulating waveform that approximates band-limited noise. In this technique, the switching regulator clock shifts from one frequency to another in a pseudorandom fashion. Since the switcher's output ripple is amplitude modulated by a noise-like signal, the output looks essentially as if there were no modulation and the downstream system implications are negligible. The higher the rate of frequency shifting, or the hop-rate, the less time the switcher is operating at a given frequency and the less time EMI will be "in-band" for a given receiver.

There is a limit, however, to the rate of frequency change (dF/dt) that the switcher can track. If the frequency abruptly hops from one frequency to another, output spikes will occur at the clock frequency transition edge (much like a load step response). Lower bandwidth switchers have more pronounced spikes. For this reason, Linear Technology's newest SSFM oscillator, the LTC6908, includes a proprietary tracking filter to smooth the transition from one frequency to the next. Most switchers have a bandwidth of 1/10th to 1/20th of the nominal switching frequency and will operate fine using the LTC6908's default modulation rate of 1/16th of the nominal clock frequency. For limited bandwidth switchers, the LTC6908's modulation rate can be decreased to 1/32nd or even 1/64th of the nominal clock rate to ensure proper regulation. The internal filter tracks the hop rate to provide optimal smoothing for all frequencies and modulation rates.

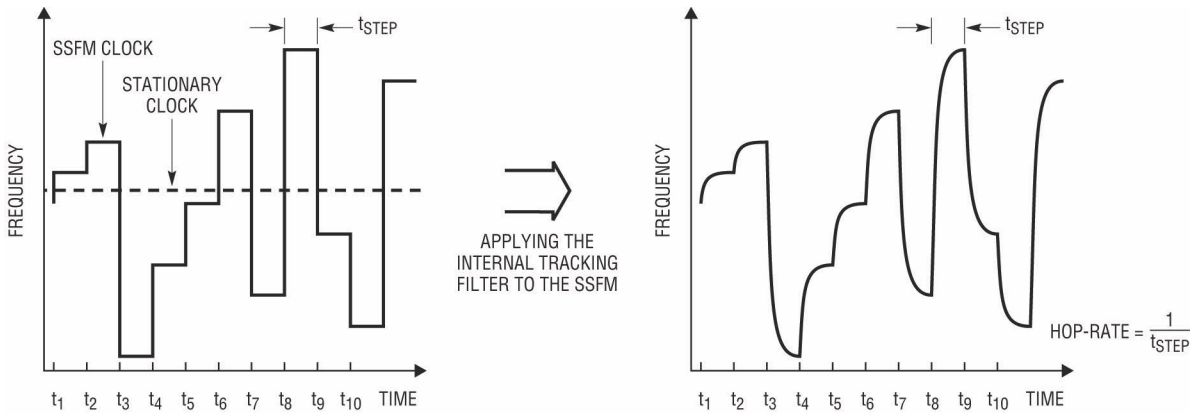

Figure 2. Pseudorandom Modulation and the LTC6908 Internal Tracking Filter

Does It Really Work?

In the world of EMC (Electromagnetic Compatibility), switchers are almost always emitters and everything else is a potential receiver. At any instant in time, peak emissions from a switching regulator *appear* to be the same, whether or not SSFM is enabled. The amplitude of the instantaneous emission is unchanged but it does move around in frequency. So, how does this work? The effectiveness of SSFM depends on the amount of spreading and the frequency modulation rate relative to the bandwidth of the receiver. To receive an "instantaneous snapshot" of emissions requires a receiver that has infinite bandwidth and, fortunately, every practical system has a limited bandwidth. A system's bandwidth determines two important characteristics: the range of frequencies for which the receiver will respond and how quickly the receiver will respond (its response time) when subjected to EMI. If the emitting signal stays in-band for a short time, relative to the system's response time, interference is significantly reduced. Any performance enhancement must be determined on a system to system basis and while SSFM may yield improvements, it is

Linear Technology's Spread Spectrum Silicon Oscillators

Device	LTC6902	LTC6908-1	LTC6908-2
Frequency Output	5kHz to 20MHz	10kHz to 10MHz	10kHz to 10MHz
Frequency Set	Resistor	Resistor	Resistor
Outputs	4	2	2
Output Phases	0°/180°/0°/180° 0°/120°/240°/NA 0°/90°/180°/270° (Programmable)	0°/180° (Fixed)	0°/90° (Fixed)
Spread Spectrum Amount	0% to 100% (Programmable)	0% or ±10% (Programmable)	0% or ±10% (Programmable)
Modulation Tracking Filter		✔	✔
Operating Temperature	-40°C to +85°C	-40°C to +125°C	-40°C to +125°C
Package	MSOP-10	SOT23, 2mm x 3mm DFN	SOT23, 2mm x 3mm DFN
Price	$2.20	$1.65	$1.65

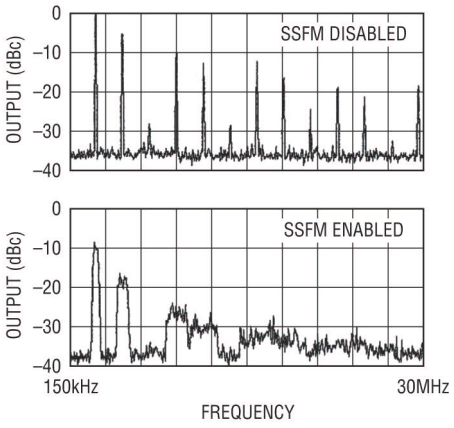

Figure 3. Switching Regulator Output Emissions using an LTC6908 (9kHz Resolution Bandwidth, Peak Detector Test)

not a substitute for standard layout, filtering and shielding practices.

In addition to in-system Electromagnetic compatibility (EMC) concerns, all systems are required to pass regulatory agency EMC tests before they are allowed for sale in the market. During regulatory agency EMC testing, the bandwidth of the test equipment is set to strictly defined standards (per CISPR 16-1) chosen to reflect the real world bandwidths of interest. The regulatory agency measurement bandwidths are well defined and consistent for all systems. Just as discussed in the previous paragraph, if the emitting signal enters the measurement system's band infrequently and for a short duration, relative to the system's response time, measured EMI is reduced.

Summary

In applications using multiple switching regulators, multiphase synchronization offers clear benefits, including reduced EMI. As for the EMI benefits of SSFM, it depends on the bandwidths of interest. SSFM is not a substitute for proper design, but when faced with unacceptable EMI at the end of a design, few options are as straightforward as enabling SSFM on the switching regulator clock. Using Linear Technology's LTC6908, both multi-phase synchronization and SSFM could hardly be simpler. The amount of frequency spreading and the phase relationship between outputs is fixed and the user only needs to program the center frequency and select one of three modulation rates. With a price of $1.65, the small size, simplicity and potential benefits make the LTC6908 very affordable insurance.

LTC6908 SSFM Clock (2mm x 3mm DFN Package)

Regulatory Testing

Regulatory agency EMC tests first scan each band using an envelope detector called a peak detector. Measurements of the peak detector that are above the pass/fail limit are further analyzed with a quasi-peak detector. The quasi-peak detector processes the peak detector's output to weigh the signal measurement according to its repetition rate. Additionally, many agencies require that a system pass a test using an average detector. The average detector is simply the peak detected output processed through a very low frequency, low pass filter. Note that a continuous, steady state, stationary emission will yield the same measurement regardless of which detector is used.

Using SSFM, if the finite response time of the measurement system is longer than the time for which emissions are in band, the peak detector measurement will be reduced. The typical bandwidth setting of the detector results in a modest amount of attenuation. With SSFM, the quasi-peak and average detector measurements can be even lower and never results in a higher value. Typically, SSFM provides a modest reduction of the quasi-peak detector measurement and a considerable reduction of the average detector measurement. In summary, SSFM potentially lowers the peak detected measurement by staying in the measurement band for short periods of time, gives an additional quasi-peak detector improvement by entering the measurement band infrequently and yields even more substantial improvement with the average detector.

Regulatory Agency EMI Test Bandwidths (per CISPR 16-1)	
Band A (9KHz to 150kHz):	BW = 220Hz
Band B (150kHz to 30MHz):	BW = 9kHz
Band C (30MHz to 1000MHz):	BW = 120kHz
Real World System Bandwidths	
Voice:	BW = 3kHz
GSM:	BW = 8kHz
AM Radio:	BW = 9kHz
Audio:	BW = 20kHz
FM Radio:	BW = 75kHz
TV:	BW = 6-8 MHz

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Reducing ground bounce in dc/dc-converter applications

ELECTRICAL GROUND, WHICH LOOKS SIMPLE ON A SCHEMATIC, CAN BECOME COMPLEX DEPENDING ON HOW YOU LAY OUT THE PC BOARD. UNFORTUNATELY, GROUND-NODE ANALYSIS IS DIFFICULT. HOWEVER, UNDERSTANDING THE PHYSICS OF GROUND NOISE HELPS TO REDUCE THE PROBLEM.

"Ground bounce" is the amount that a ground return rises or falls relative to the system's 0V reference, and, in a dc/dc-switching converter, ground bounce can be many volts, often because of changing magnetic flux. Magnetic flux is proportional to a magnetic field that passes through a loop area. **Figure 1** illustrates magnetic flux in a simple circuit loop. A voltage source pushes current through a resistor and around a loop of wire. Imagine that you are grabbing the wire with your right hand. Pointing your thumb in the direction of current flow, your fingers wrap around the wire in the direction of the magnetic-field lines. As those field lines pass through the loop, they establish magnetic flux. If you change either the magnetic-field strength or the loop area, the flux will change, inducing a voltage in the wire. **Figure 2** shows the same circuit with an added switch. When the switch opens, current stops flowing, so the magnetic flux collapses, inducing a voltage everywhere along the wire.

Generally, pc-board-ground-plane resistance is a less important source of ground bounce than magnetic-flux change. (The sheet resistance of 1-oz copper is about 500 μΩ/□, so a 1A change in current produces 500 μV/□ of bounce—a problem for thin, long, or daisy-chained grounds or precision electronics.) Parasitic capacitance is a path for large transient currents to a ground return. The change in magnetic flux from those current spikes induces ground bounce. Therefore, the best way to reduce ground bounce in a switching dc/dc converter is to control changes in magnetic flux.

In a basic circuit, output current remains constant, but the loop area changes (**Figure 3**). In **Figure 3a**, ideal wires connect an ideal voltage source to an ideal current source. Current flows in a loop that includes ground return. In **Figure 3b**, the switch changes position. The current source is still dc, but the loop area changes and generates a magnetic-flux change, inducing a ground-bounce voltage (see **sidebar** "Five pc-board-layout configurations affect ground bounce").

BUCK-CONVERTER GROUND BOUNCE

The buck converter in **Figure 4** is similar to the simple circuit in **Figure 3**. At high frequencies, a large capacitor, such as a buck input capacitor, looks like a dc voltage source. Similarly, the large output buck inductor looks like a dc current source. Magnetic flux changes as the switch moves between the posi-

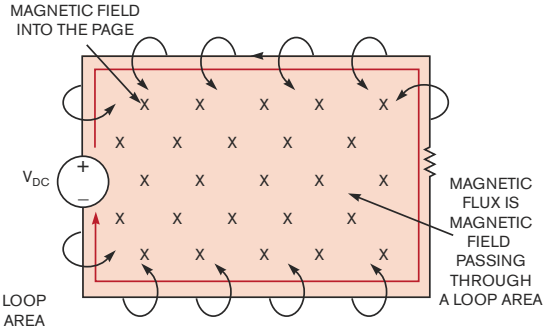

Figure 1 Magnetic flux is proportional to the magnetic field passing through a loop that a circuit forms.

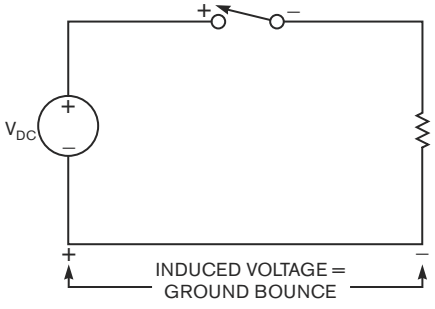

Figure 2 When the formerly closed switch in this simple circuit opens, the magnetic flux goes to zero, inducing a voltage along the circuit.

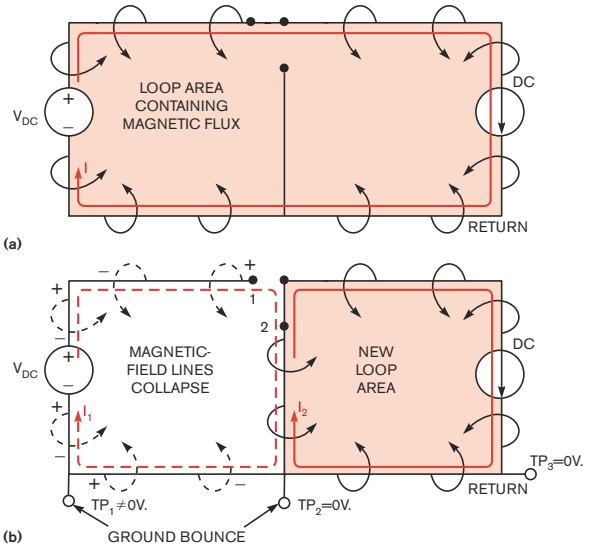

Figure 3 The area of the loop changes based on whether the switch is in position 1 or 2 (a). The collapse of the magnetic field as I_1 goes to zero induces a voltage (b).

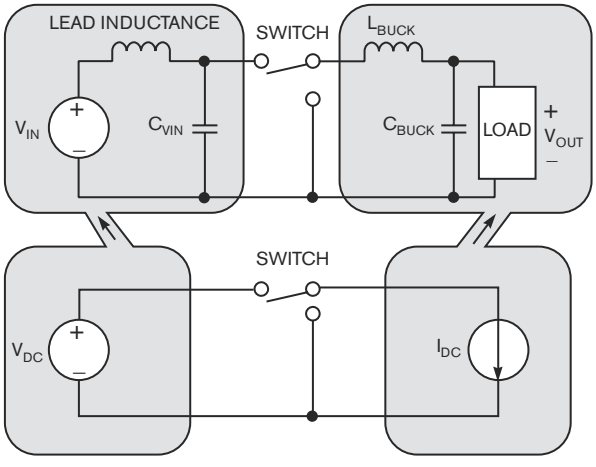

Figure 4 A high-frequency switch sees a large C_{VIN} as a voltage source and a large buck inductor as a current source.

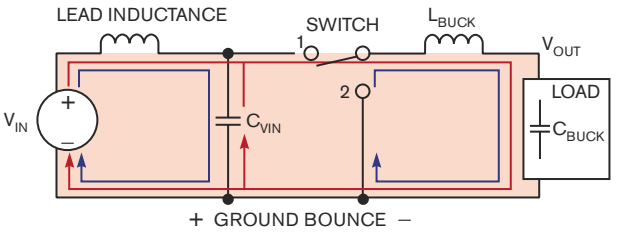

Figure 5 In this simple buck converter, the red current loops indicate the switch in Position 1, and the blue loops indicate the switch in Position 2.

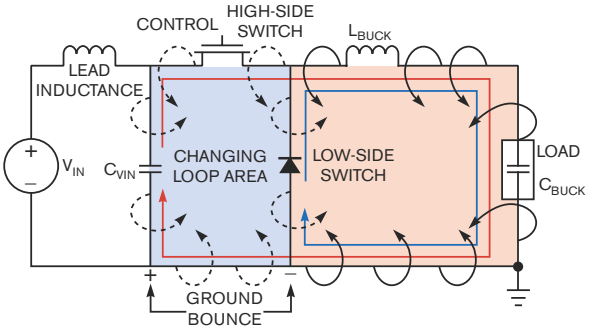

Figure 6 A switching power semiconductor replaces the simplified switch of Figure 5.

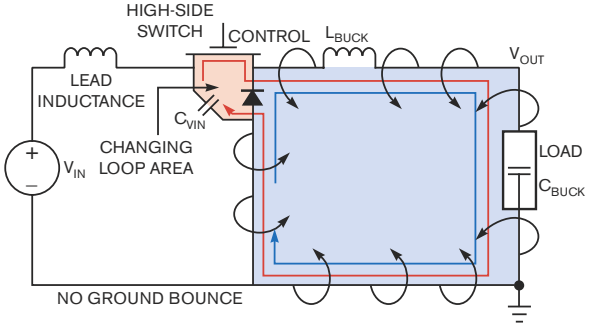

Figure 7 C_{VIN} bypasses the top of the high-side switch to the bottom of the low-side switch, shrinking the changing-loop area and greatly reducing ground bounce.

tions (**Figure 5**). The large buck inductor, L_{BUCK}, holds the output current roughly constant. Similarly, C_{VIN} maintains a more or less constant voltage across the parasitic-input inductance, so the input current is also approximately constant. Although the input and output currents are roughly dc, as the switch moves from Position 1 to Position 2, the total loop area rapidly changes in the circuit's middle. This change means that magnetic flux is changing, which in turn induces ground bounce along the return wire.

Buck converters comprise semiconductor switches (**Figure 6**). But, as the complexity increases, the analysis of ground bounce that changing magnetic flux induces remains simple and intuitive. Knowing that a change in magnetic flux induces voltage everywhere along a ground return brings up an interesting question: Where is true ground? After all, ground bounce means a ground-return trace is bouncing with respect to ground, and you must identify that point.

In the case of power-regulation circuits, true ground needs to be at the point of load. A dc/dc converter delivers quality voltage and current to the load. All other points returning current are not grounds but just return lines to ground. **Figure 7** shows how careful placement of C_{VIN} reduces ground bounce. Capacitor C_{VIN} bypasses the top of the high-side switch to the bottom of the low-side switch, shrinking the changing-loop area. Additionally, the changing-loop area is isolated from the ground return. From the

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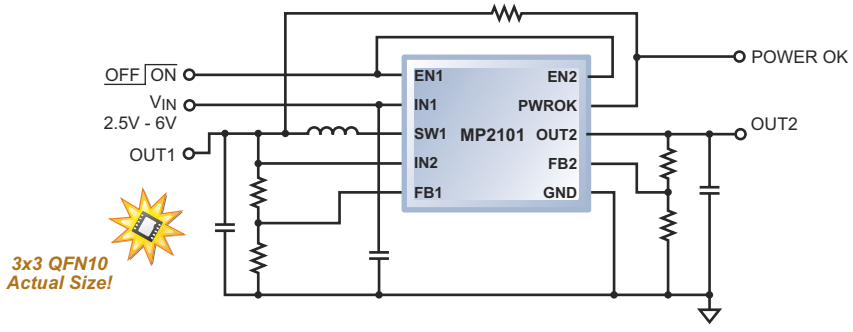

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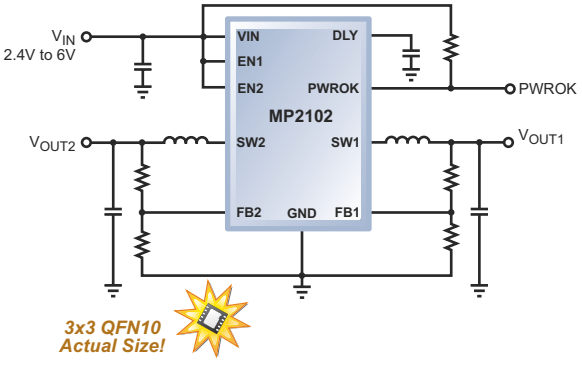

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ground of V_{IN} to the true ground of the load, no loop area or switch-current changes flow from one case to the next. Consequently, ground return does not bounce.

Figure 8 shows an inferior but perhaps typical pc-board layout of the buck schematic in **Figure 6**. In **Figure 8**, the high-side switch is on, and dc current flow follows the outer red loop. The low-side switch is on, and dc current flow now follows the blue loop. Note the changing loop area and, hence, the changing magnetic flux. So, this arrangement induces

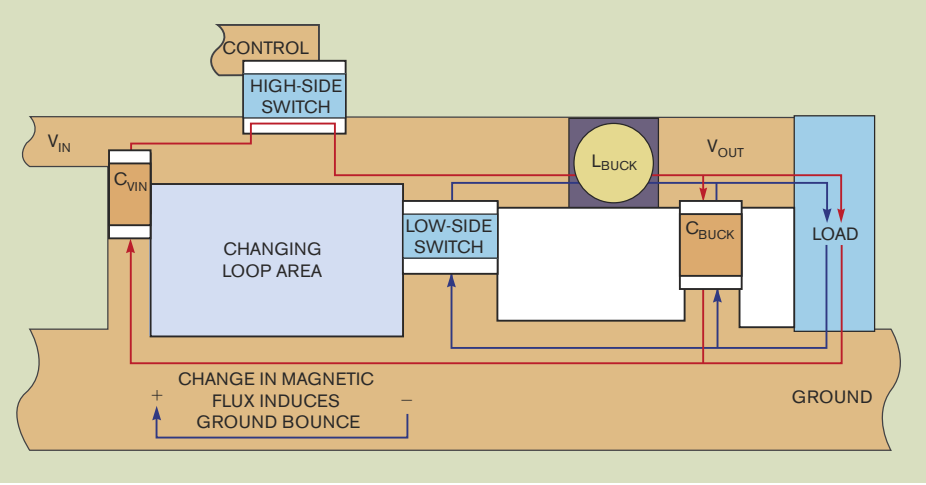

Figure 8 A bad layout causes a large change in current-loop area.

PC-BOARD-LAYOUT CONFIGURATIONS AFFECT GROUND BOUNCE

Conductors that cross at right angles do not interact magnetically: The magnetic field from the vertical trace induces positive and negative voltages that cancel in the horizontal trace (Figure A).

Magnetic-field lines around parallel wires with equal currents cancel everywhere between the wires, so the total stored energy is less than what you would find for the individual wires. Wide pc-board traces have less inductance than narrow traces (Figure B).

Magnetic-field lines around parallel conductors with opposite current flow cancel everywhere outside the conductors and add everywhere inside. If you make the inside loop area small, then the total magnetic flux and, therefore, the inductance will also be small (Figure C). This behavior is the reason that the ac ground-plane return current always flows under the top-trace conductor.

Corners have more inductance because both the vertical and horizontal traces see a magnetic field from themselves as well as from the perpendicular trace (Figure D). A current flows into a top trace, down a via, into a ground plane, and back up a via to the bottom of the source (Figure E). The return current flows, with dc current taking the path of least resistance and ac current taking the path of least impedance. Because top-trace corners and ground-plane cuts increase impedance, you can expect ground bounce. The change in magnetic flux at those points induces the bounce.

The upper trace in Figure F shows good layout practice; the capacitor is in line with the current flow, creating a minimal loop size. The bottom trace, with the capacitor at right angles to the current flow, creates an unnecessarily large loop, resulting in ground bounce.

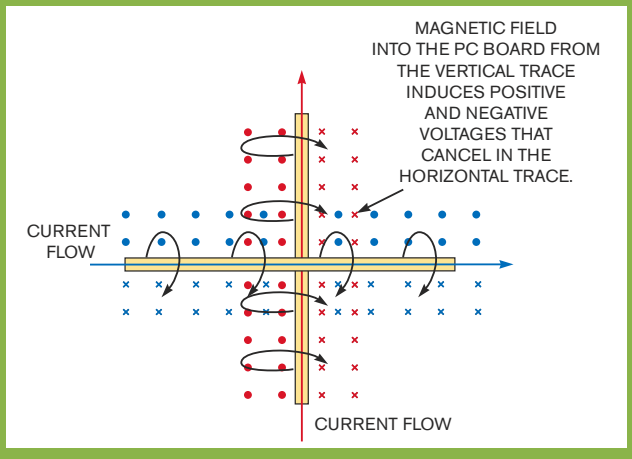

Figure A The magnetic field from the vertical trace induces positive and negative voltages that cancel in the horizontal trace.

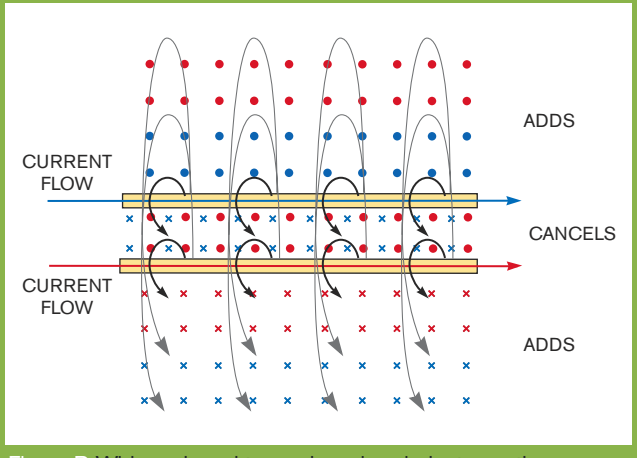

Figure B Wide pc-board traces have less inductance than narrow traces.

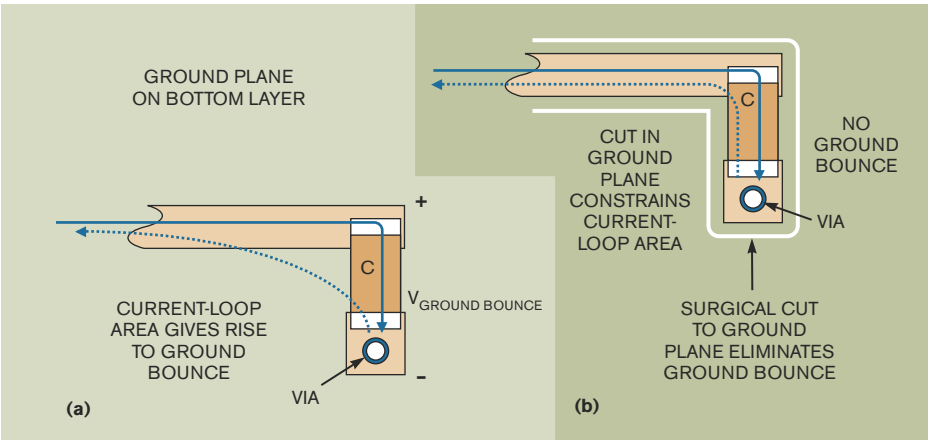

Figure 9 The ground plane is solid and uncut, and the top-trace current flows through the capacitor, down the via, and out the ground plane (a). A careful cut in the ground plane constrains the return current to a minimum-loop area and fixes the bounce (b).

voltage, and the ground bounces. **Figure 9** provides an example in which a solid ground plane may be a poor choice. In this case, designers constructed a two-layer pc board so that a bypass capacitor attaches at a right angle to a top-layer supply line. In **Figure 9a**, the ground plane is solid and uncut, a common but sometimes poor layout practice. Top-trace current flows through the capacitor, down the via, and out the ground plane.

Because ac current always

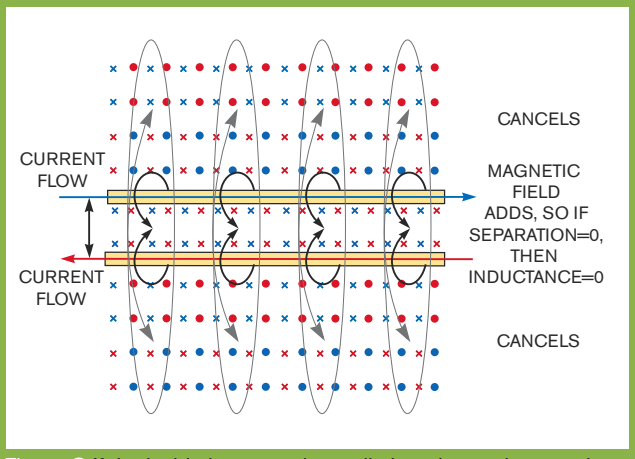

Figure C If the inside loop area is small, then the total magnetic flux and, therefore, the inductance will also be small.

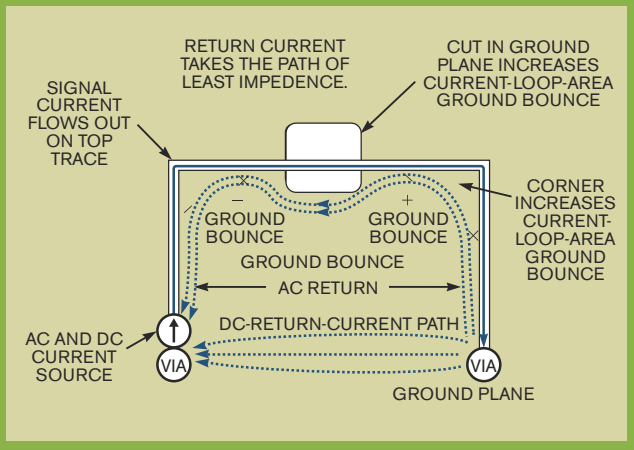

Figure E A current flows into a top trace, down a via, into a ground plane, and back up a via to the bottom of the source.

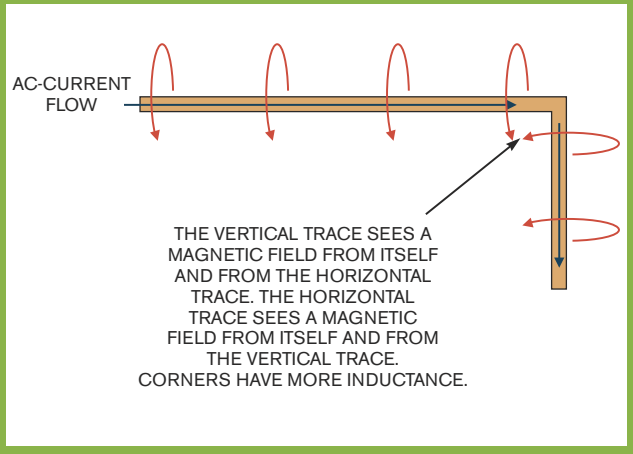

Figure D Both the vertical and horizontal traces see a magnetic field from themselves as well as from the perpendicular trace.

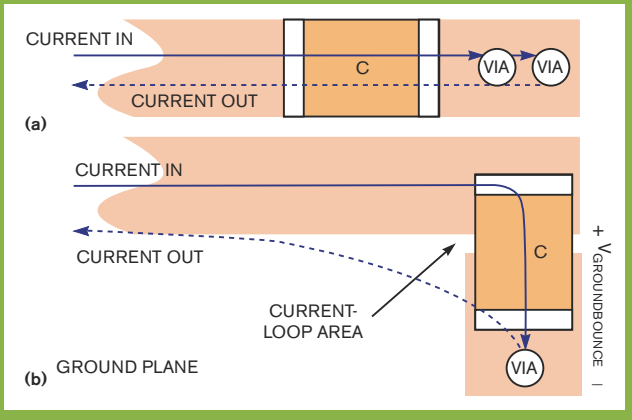

Figure F In good layout practice, the capacitor is in line with the current flow, creating a minimal loop size (a). Having the capacitor at right angles creates a large loop, causing ground bounce (b).

takes the path of least impedance, ground-return current cuts the corner on its way back to the source. But the current has a magnetic field and draws out a loop area that changes with a change in current magnitude or frequency. Magnetic flux is in that loop and changes if either the current magnitude or the frequency changes. That change means that a sheet ground plane—even if it's superconducting—can bounce. However, a careful cut in the ground plane constrains the return current to a minimum loop area and fixes the bounce. This approach also isolates the cut return line's bounce voltage from the general ground plane.

The pc-board layout in **Figure 10** uses the same principle as the one in **Figure 9** to reduce ground bounce. Designers built a two-layer pc board's input capacitor and both switches over an island in the ground plane. This layout is not necessarily the best, but it works well and illustrates the key principles. Note the large loop areas traced out by the red and blue current paths in **Figure 10**. But the two loops differ only slightly. The small change in loop area means a small change in magnetic flux and, hence, a small ground bounce. Additionally, in the ground-return island in which magnetic fields and loop area do change, the cut contains any ground-return bounce. Also, the input capacitor, C_{VIN} (**Figure 10**), may look as if it resides in a different area from the high- and low-side switches from C_{VIN} in **Figure 7**, but it is actually electrically nearby. Physical proximity can be good, but the electrical proximity that you achieve by minimizing the loop area is more important.

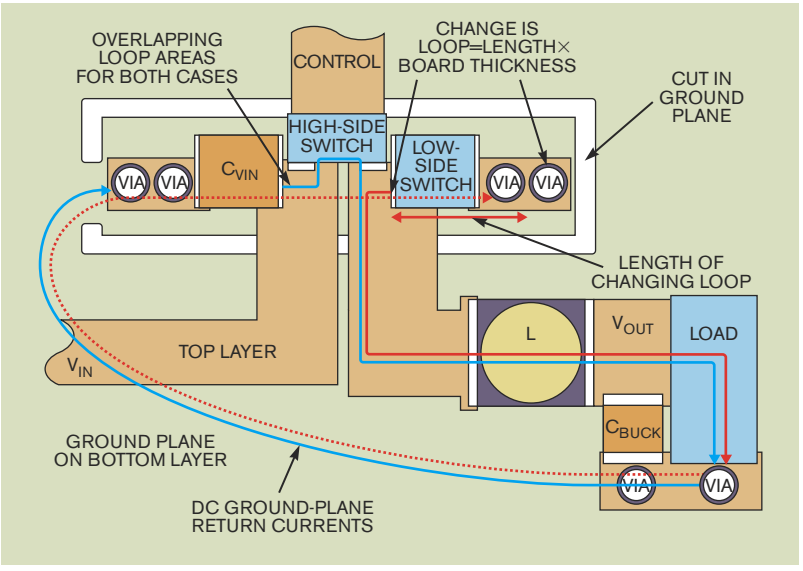

Figure 10 Designers built a two-layer pc board so that the input capacitor and both switches are over an island in the ground plane. Although the loop area by the red and blue currents is large, the difference between the two loops is small. The small change in loop area means a small change in magnetic flux and a correspondingly small ground bounce.

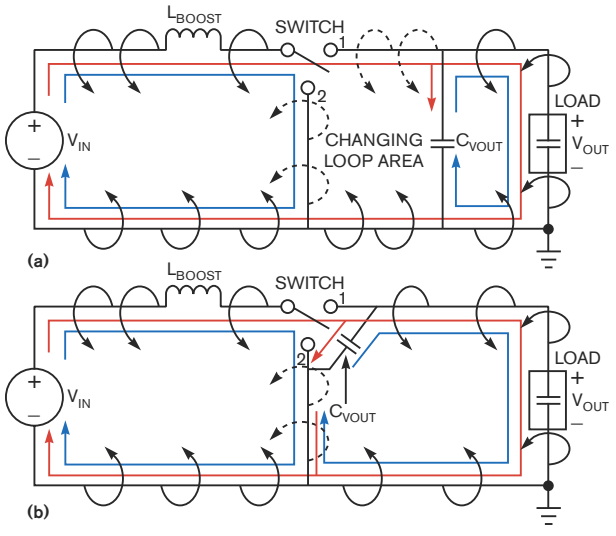

Figure 11 Unlike in a bad design (a), you must place the boost converter's output capacitor from the top of the high-side switch to the bottom of the low-side switch to minimize the change in loop area (b).

BOOST-CONVERTER GROUND BOUNCE

A boost converter is the inverse of a buck converter, so you must place the output capacitor so that it goes from the top of the high-side switch to the bottom of the low-side switch to minimize the change in loop area (**Figure 11**). Ground bounce results primarily from a change in magnetic flux, which induces a ground-bounce voltage. In a dc/dc-switching power supply, the flux changes because high-speed switches direct current to different current-loop areas. However, careful placement of the buck/boost-input/output capacitor and a surgical cut to a ground plane can isolate bounce. Be careful when cutting a ground plane, because doing so can increase the loop area for some other return current in the circuit. EDN

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AUTHOR'S BIOGRAPHY

Jeff Barrow is a design manager for the Display Technology Products Group at Analog Devices (Tucson, AZ), where he is responsible for the development of multichannel power ICs and analog-signal conditioners for LCD TVs and monitors. He received a bachelor's degree in electrical engineering from the University of Arizona (Tucson), and his personal interests include physics and electronics.

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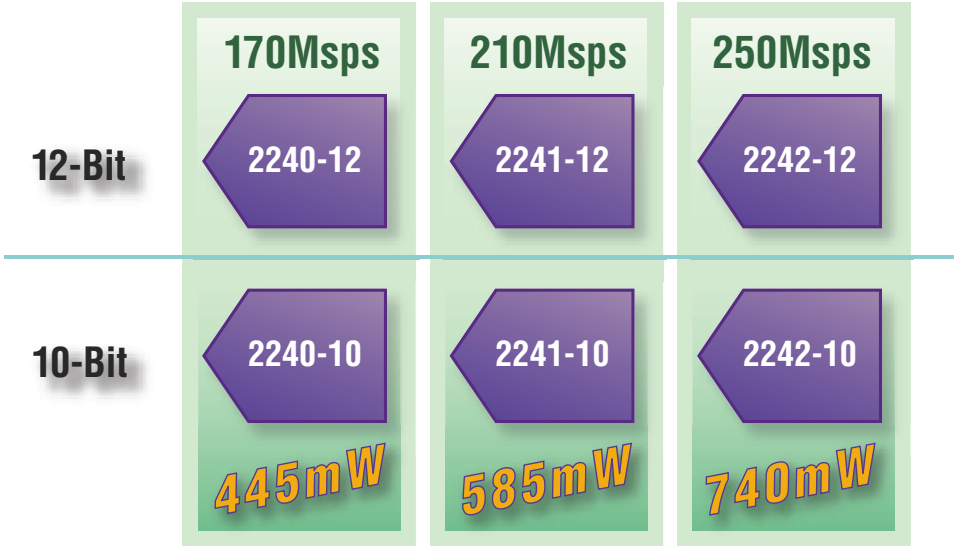

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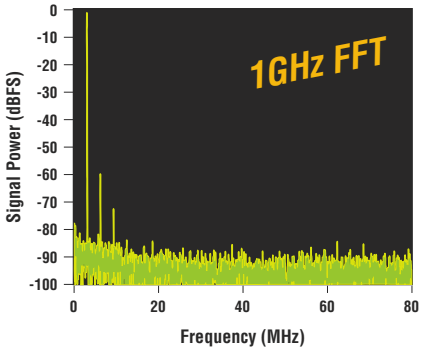

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DESIGN NOTES

High Voltage Buck Converters Drive High Power LEDs

Design Note 392

Keith Szolusha

Introduction

High power LEDs continue to replace traditional bulbs in new automotive, industrial, backlight display and architectural detail lighting systems. LEDs excel in a wide range of performance and cost parameters, including excellent spectral performance, long life, robustness, falling manufacturing cost and relatively safe materials. Linear Technology offers a large and growing family of high voltage DC/DC converters tailored specifically to drive high-powered LEDs.

The LT®3474 and LT3475, for example, are high voltage, high current, single- and dual-channel buck LED converters with wide PWM dimming ratios that can drive one or more LEDs up to 1A and 1.5A for 80 lumens to 120 lumens per LED (or more as higher output LEDs become available). These dedicated LED drivers have onboard high voltage NPN power switches and internal sense resistors to minimize board space, reduce component count and simplify design.

With their high side sense resistors, the LT3474 and LT3475 can drive LEDs tied to ground, an important advantage in many systems. Current-mode control and a precise reference voltage optimize loop dynamics for a well regulated, low ripple constant LED current. Thermally enhanced exposed pad packages keep the junction temperature low during high power operation in stressful environments. A PWM pin uses the dimming MOSFET gate signal to extend the dimming ratio of the converter by maintaining constant output capacitor voltage and control loop state during PWM dimming off-time. Shutdown and external analog current adjust pins provide simple interface for further LED light and current control flexibility in any system.

Single Buck 1A LED Driver

The LT3474 buck converter 1A LED driver shown in Figure 1 has features that suit it to automotive applications (and other battery-powered applications) or to industrial applications with limited board space, high voltage and high ambient temperature. This scheme uses a high side integrated 100mΩ sense resistor for true LED current sensing and regulation, superior to the common and less efficient method of biasing LEDs with a constant voltage and a power wasting bias resistor.

The 4V to 36V input voltage range makes it ideal to use with little-to-no input transient protection circuitry in automotive, industrial and avionic applications where long cables from the battery result in very high input spikes.

The boosted NPN power switch results in high efficiency for both 1- and 2-LED applications (Figure 2). The boost diode is integrated to further reduce component count. Driving the shutdown pin to ground turns off the LEDs and reduces the input current to less than 2µA for battery longevity.

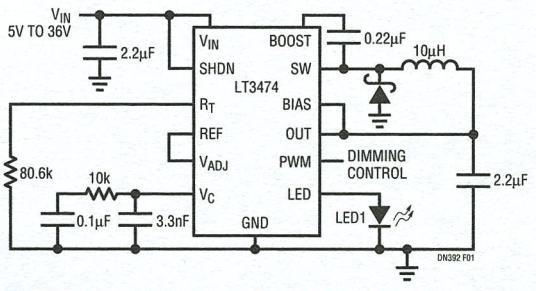

Figure 1. LT3474 High Voltage Buck LED Driver Regulates 1A

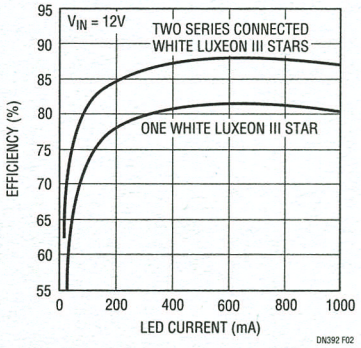

Figure 2. LT3474 Buck Drives Single or Multiple LEDs with High Efficiency

LED brightness is controlled by either the 400:1 True Color PWM™ dimming with an external MOSFET driver or with an analog 25:1 (or filtered PWM) signal on the V_{ADJ} pin. Applications can be optimized for highest efficiency or smallest component size via an external resistor that programs the switching frequency from 200kHz to 2MHz.

The maximum output voltage of the LT3474 is clamped at 13.8V which protects the LT3474 output from LED open circuit. Short-circuit protection is the final detail that makes the LT3474 a bulletproof converter in the case of all types of LED failures.

Dual Buck 1.5A LED Driver

Figure 3 shows a dual-channel 1.5A buck converter LED driver using the LT3475 which is essentially two LT3474 converters combined in a single IC with a few additional features. This simple solution is ideal for automotive applications where two overhead or dashboard lights are needed in the same system. Both light channels (each a single or a string of LEDs) have separate V_{ADJ} voltages and PWM signals for independent operation, but a single shutdown pin further improves battery-saving micropower operation by reducing the total battery drain of the circuit to 2µA in shutdown.

Each of the dual outputs can be driven as high as 1.5A for more powerful LEDs or LEDs that require higher current and less forward voltage such as red and amber brake and signal LEDs. Although the maximum output voltage is clamped at the same level as the LT3474 at 13.8V, the maximum power output capability of the LT3475 is three times higher. The PWM dimming ratio is also greater—1200:1 or higher with the extended dimming ratio circuit in Figure 4. Improvements in PWM dimming techniques with lower minimum dimming on-time requirements help this IC achieve extreme automotive and nighttime dimming levels while maintaining the same true color as 100% duty cycle. Independent analog V_{ADJ} dimming ratio is 30:1 (50mA LED current) for each channel. To reduce internal power dissipation, the boost diode for each channel is left out of the IC.

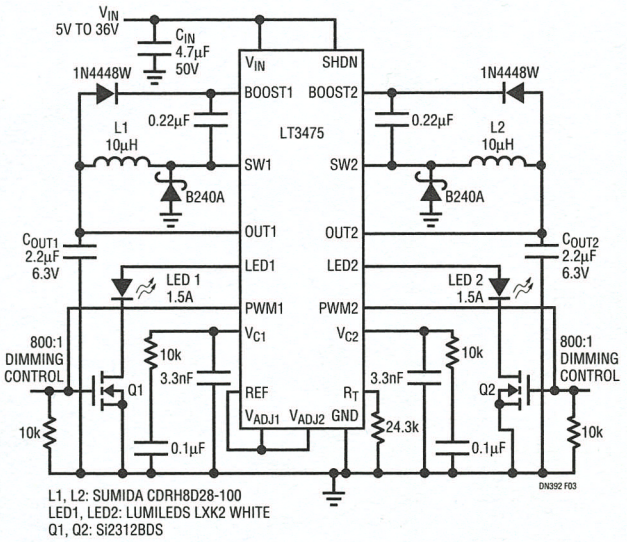

Figure 3. LT3475 Dual High Voltage Buck LED Driver Regulates 1.5A

Compared to the LT3474, the LT3475 offers three times the power capability, the same shutdown current, the same switching frequency range, a slightly higher input voltage (36V operating, 40V maximum), a higher dimming ratio, a higher LED current and only a slightly bigger package (20-pin versus 16-pin exposed thermal pad TSSOP)—making it a great choice for higher power solutions. In addition, the anti-phase switching of the two channels in the LT3475 reduces the input ripple seen by the source and limits the need for extra high voltage input capacitors.

Conclusion

The LT3474 and LT3475 are excellent choices for high voltage, high current, buck LED drivers in automotive, industrial, backlight display and architectural display lighting systems. The heavily integrated ICs reduce component count and board space, while still providing flexible features such as adjustable LED current, PWM dimming and adjustable operating frequency. Accurate LED current regulation makes these ICs superior to other DC/DC voltage regulators or LED drivers. Efficiency as high as 88% combined with less than 2µA of shutdown current save battery power and extend lifetime.

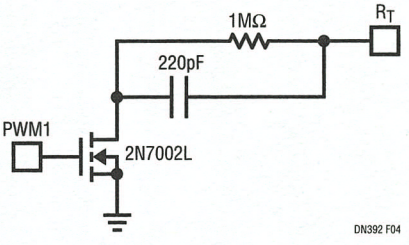

Figure 4. LT3475 Extended Dimming Range Circuit Provides 1200:1 PWM Dimming Ratio When Added to Figure 3, and Up to 3000:1 at 1.4MHz

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Error compensation improves bipolar-current sinks

Christian de Godzinsky, Planmeca Oy, Helsinki, Finland

You can improve a current sink's accuracy by at least two orders of magnitude by adding two standard 1%-tolerance resistors. As a bonus, you also compensate for errors that a low-current-gain pass transistor's base current introduces. To do so, you measure the transistor's base current and add a proportionally scaled error term to the source's reference voltage. When you design a current sink, you can use a MOSFET for the sink's pass transistor because of its nearly infinite power gain and low gate current. However, a high-power MOSFET presents high input and output capacitances that reduce the sink's high-frequency output impedance.

As an alternative, a low-current-gain, bipolar power transistor presents a much lower output capacitance than does a MOSFET of comparable power ratings. **Figure 1** shows a design for a bipolar-transistor-based current sink that unfortunately suffers from accuracy errors due to Q_1's base current's flowing into the current-measurement resistor R_1. The base current varies with changes in Q_1's collector current and current gain, which in turn depend on Q_1's production tolerances, junction temperature, and collector-emitter voltage.

You can use a Darlington transistor to increase the circuit's current gain and reduce the output error, but few Darlington transistors offer good high-frequency parameters. Superbeta power transistors are rare, have typically lower unity-gain-bandwidth frequencies, and are more expensive. In other words, even though a bipolar transistor presents higher output impedance at high frequencies, the error from its base current makes it a poor choice for a high-precision current sink. You could compensate for base-current errors by measuring the output transistor's collector current and introducing a correction factor, but that approach increases circuit complexity and reduces the sink's output impedance.

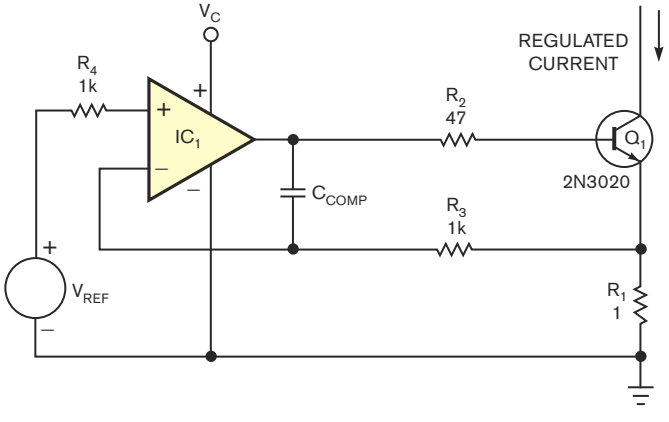


Figure 1 This typical quickly responding constant-current sink uses a bipolar transistor but suffers from base-current-induced error. Its nominal output current is $I_{OUT}=(V_{REF}/R_1)-I_B$.

Figure 2 shows a better approach, which adds a differential amplifier, IC_2, and resistors R_6 through R_9 to measure Q_1's base current by sampling the voltage across R_2. Resistors R_4 and R_5 scale and sum the error and reference voltages you apply to differential amplifier IC_1. Because IC_1's inverting input connects to current-shunt resistor R_1's upper end and not to ground, the reference voltage, V_{REF}, determines the error voltage applied to Q_1, preserving output scaling and allowing output-current calculation as V_{REF}/R_1. As a result, the regulated voltage across R_1 represents the sum of the desired output current plus the transistor's base current. Because the transistor inherently "subtracts" its base current, its collector current and, hence, the output current have no base-current error.

You can simplify the circuit and preserve its error-correction properties by combining IC_1 and IC_2; better yet, you can add two resistors to **Figure 1** to

achieve the same effect. **Figure 3** shows the final circuit. To understand its operation, think of the circuit as a voltage regulator that delivers a voltage equal to V_{REF} across R_1. If you short-circuit base resistor R_2, note that any common-mode error that resistors R_5 and R_6 introduce cancels and thus has no effect on Q_1's base voltage. When you feed the voltage drop back to IC_1's input through R_5 and R_4, the voltage drop across R_2, representing Q_1's base current, increases the regulated voltage across R_1 by the ratio of R_5/R_4. If the ratio of R_5/R_4 equals that of R_2/R_1, the voltage across R_1 includes an error term that effectively cancels the base current. If $R_3=R_4$ and $R_5=R_6$, the following **equation** describes the output current, I_{OUT}:

$$I_{OUT}=\frac{V_{REF}+I_B\times R_2\times\frac{R_4}{R_5}}{R_1}-I_B.$$

Because the base current, I_B, appears twice with opposite signs and cancels, the equation simplifies to: $I_{OUT}=(V_{REF}/R_1)$.

To optimize the circuit's performance, use the following resistor ratios: $R_2/R_1=R_5/R_4$, $R_5=R_6$, $R_3=R_4$, $R_5>>R_4$, and $R_3>>R_1$. Using standard 1%-tolerance resistors in the circuit of **Figure 3** reduces the error from Q_1's base current to about one-one-hundredth of its uncompensated level. Without compensation, a low-gain power transistor with a typical current gain of 25 at Q_1 would introduce a full-scale current error of 4%. The circuit corrects the error to 0.04% and raises Q_1's current gain to an effective current gain of 2500. Perfect matching would result in an immeasurably small base-current error. Note that IC_1's input common-mode-voltage range must include the negative-supply-voltage rail. Equal resistances at both of IC_1's inputs balance the op amp's input-bias currents. The minimum power-supply voltage depends on IC_1's maximum current-sourcing capability and on the sum of the worst-case voltage drops across Q_1's base-emitter junction, R_1 and R_2. The circuit's maximum output current depends on Q_1's worst-case minimum current gain times IC_1's worst-case minimum output current.

To ensure stable operation, use a unity-gain-stable op amp for IC_1. When the circuit operates within its nominal current range, an op amp whose response time is substantially

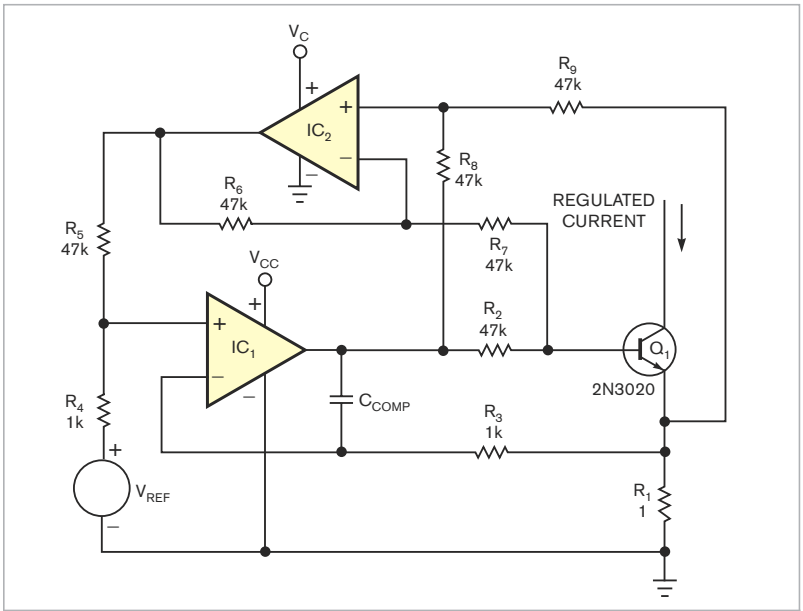


Figure 2 Adding base-current error compensation improves the circuit's performance. Using perfectly matched resistors simplifies the output-current equation to $I_{OUT}=(V_{REF}/R_1)$.

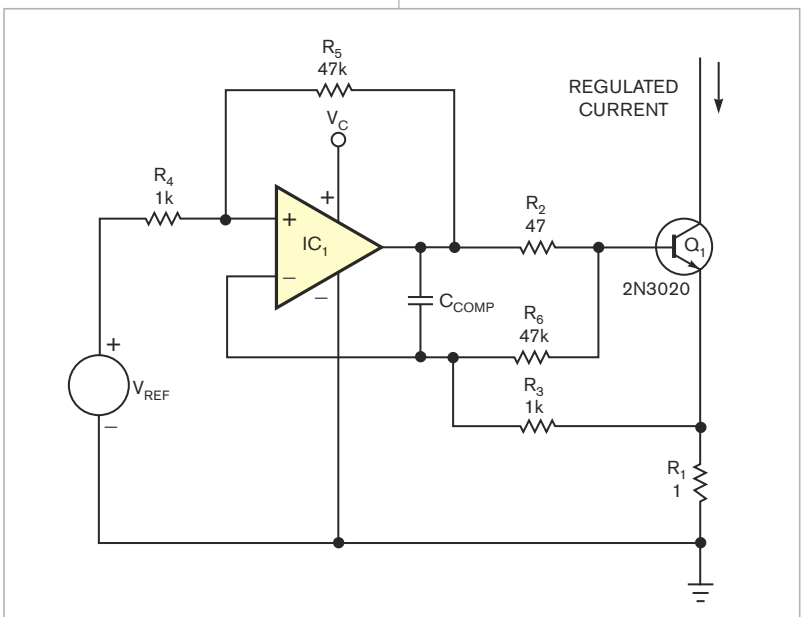
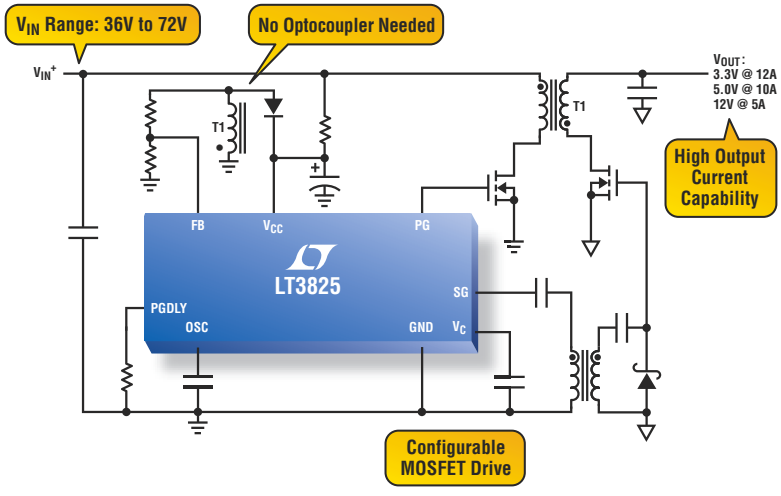
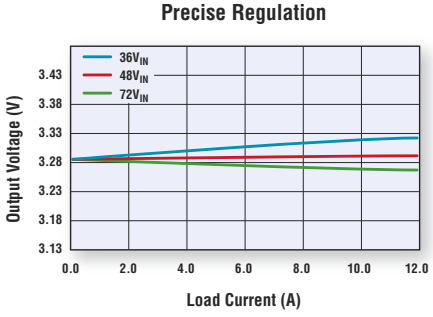


Figure 3 You can further simplify the current sink's design by adding only two resistors, R_5 and R_6, to the original in Figure 1. The output-current equation remains $I_{OUT}=(V_{REF}/R_1)$, as in Figure 2.

Simple 12A Synchronous Flyback





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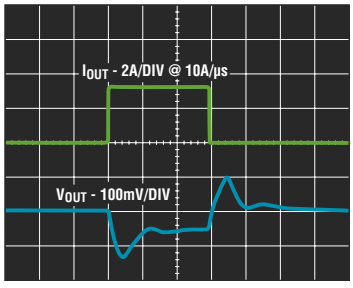

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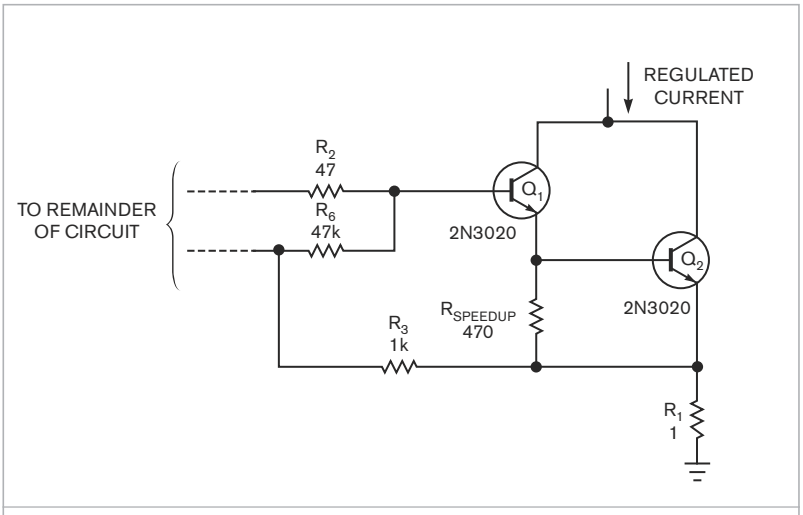

Figure 4 Adding $R_{SPEEDUP}$ improves the performance of a two-transistor Darlington output stage.

longer than Q_1's generally doesn't require installation of compensation capacitor C_{COMP}. However, a small capacitor of a few tens of picofarads guarantees stability under all conditions—for example, when the circuit's output current and the feedback voltage across R_1 approach zero.

The circuit in **Figure 3** works equally well if you use a Darlington transistor for Q_1 because its higher current gain further improves the circuit's operation. If you use two discrete bipolar transistors, you can improve the composite Darlington transistor's turn-off time by connecting a resistor between the output transistor's base and emitter to remove its excess base charge (**Figure 4**).

You can use either a fixed or an adjustable reference-voltage source, but for the smallest possible error, the reference source's output impedance should be fairly low to sink feedback current from R_4. You can also proportionally increase the values of resistors R_3 through R_6 to reduce the amount of current that the reference source absorbs. It's amazing what you can achieve by adding only two resistors to an already-simple circuit. EDN

Phase-sequence indicator uses few passive components

Metodi Iliev, University of California—Berkeley

In a three-phase ac system, a power source with three wires delivers ac potentials of equal frequency and amplitudes with respect to a zero-potential wire, each shifted in phase by 120° from one wire to the next. Two possibilities exist for establishing a phase sequence. In the first, voltage on the second wire shifts by 120° relative to the first, and, in the second, a −120° shift occurs with respect to the first wire. Phase order determines the direction of rotation of three-phase ac motors and affects other equipment that requires the correct phase sequence: a positive 120° shift. You can use a few low-cost passive components to build a phase-sequence indicator.

Figure 1 shows a conceptual circuit that can detect both phase sequences. For certain component values, the following conditions apply: The voltages across R_1 and C_2 are equal—that is, their magnitudes and phases are the same—only when V_{S2} occurs exactly 120° ahead of V_{S1}, which indicates the correct phase sequence. In this case, the voltage between points A and B is zero. Conversely, the voltages across C_2 and R_3 are equal only when V_{S2} is ahead of V_{S3} by 120°, which corresponds to a reversed sequence.

Referring to the phasor diagram in **Figure 2**, when the voltages across R_1 and C_2 are equal, $V_{C1}=-V_{R2}$, $V_{C1}+V_{R1}=V_{S1}$, and $V_{C2}+V_{R2}=V_{S2}$. The following **equations** satisfy these conditions: $|V_{R1}|=|V_{C2}|=(1/2)|V_{S2}|=(1/2)|V_{S1}|$, and $|V_{C1}|=|V_{R2}|=\cos(30°)|V_{S1}|=\cos(30°)|V_{S2}|$. You calculate the component values by

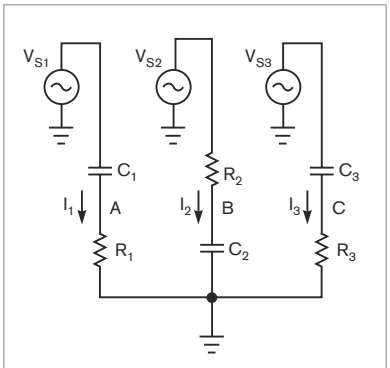

Figure 1 This conceptual circuit can detect both phase sequences.

solving the following **equations**: $|X_{C1}|=\tan(60°)\times R_1=\sqrt{3}\times R_1$, and $R_2=\tan(60°)\times|X_{C2}|$, where $X_C=-j[1/(2\pi\times f\times C)]$, and f represents the frequency of the V_S voltages.

Also, to ensure detection of a reversed phase sequence, $C_1=C_3$, and $R_1=R_3$; that is, the components in the

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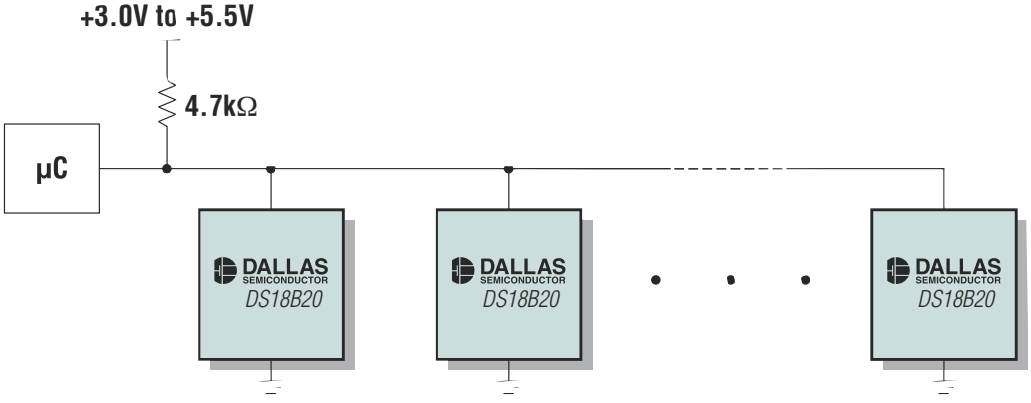

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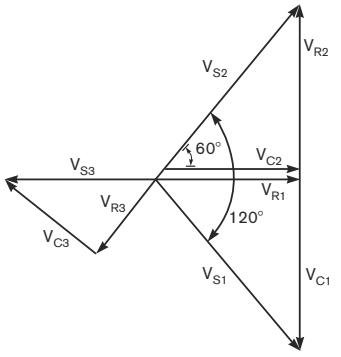

Figure 2 When the voltages across R_1 and C_2 are equal, $V_{C1}=-V_{R2}$, $V_{C1}+V_{R1}=V_{S1}$, and $V_{C2}+V_{R2}=V_{S2}$.

third branch are identical to those in the first branch. The phase-sequence-detection circuit in **Figure 3** eliminates the requirement for an accessible ground wire by adding resistors R_4 and R_5 that connect in parallel with the first and third branches. Eliminating the ground-wire requirement also dictates a ratio between $|X_{C1}+R_1|$ and $|X_{C2}+R_2|$. For no current to flow to ground from Node G, the sum of currents in the branches must equal zero, and, if you disconnect Node G from ground, its potential with respect to ground is also zero.

As long as the proportions of X_{C1} to R_1, X_{C2} to R_2, and X_{C3} to R_3 remain as noted, the balance of voltage drops remains across R_1, C_2, and R_3. Multiplying the impedance of any branch by a constant influences only the magnitude of the currents through the respective branch. The current through any branch presents the same phase angle as the voltage across a resistor in the branch. The phasor diagram in **Figure 4** shows the currents in **Figure 3**. From this diagram, if $|I_2|=\tan(60°)\times|I_1|$, then $I_1+I_2=-2\times I_3$. Thus, I_3 has half the magnitude of and an exactly opposite direction from (I_1+I_2).

A vector diagram of the currents shows that adding two currents, each with magnitudes equal to I_3 and the same phases as V_{S1} and V_{S3}, produces a summed current with the same magnitude and phase as I_3; therefore, the total current at Node G is zero: $I_1+I_2+I_3+I_1'+I_3'=I_1+I_2+2\times I_3=0$. To make the sum of the currents equal zero, $R_4=R_5=|R_1+X_{C1}|=|R_1-j[1/(2\pi\times f\times C_1)]|$. The two LEDs in **Figure 3** indicate correct or reversed-phase sequence. When LED_2 lights and LED_1 remains dark, the voltage between nodes A and B is 0V, which corresponds to a correct phase sequence. A reversed-phase sequence lights LED_1 while LED_2 remains dark. The diodes connected in parallel with the LEDs protect against exceeding the LEDs' reverse-breakdown voltages, and resistors R_6 and R_7 limit forward currents through the LEDs. For greater sensitivity, you can replace the LEDs with high-input-impedance ac-detector circuits.

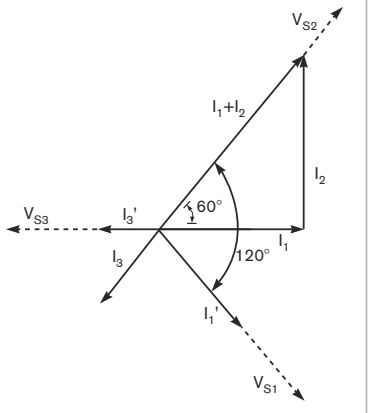

Figure 4 I_3 has half the magnitude and an exactly opposite direction to (I_1+I_2) in Figure 3.

The circuit's final version includes indicators that show whether all three phases carry voltage. In the circuit in **Figure 3**, a phase that carries 0V lights both LEDs. Depending on your application, you can connect voltage-detection circuits comprising LEDs and protection diodes in series with current-limiting resistors between V_{S1}, V_{S2}, and V_{S3} and Node G. You can also use low-wattage neon lamps with appropriate series-current-limiting resistors.

When selecting components, ensure that their values conform to the following proportions. For an arbitrarily chosen value for C_1, $R_1=R_2=R_3=1/(2\pi\times f\times C_1\times\tan(60°))$, $C_1=C_3$, $C_2=3C_1$, and $R_4=R_5=2\times R_1$. When you select a value for C_1, the currents through the detection circuitry should be significantly lower than the currents through the branches, which excludes arbitrarily low values for C_1. EDN

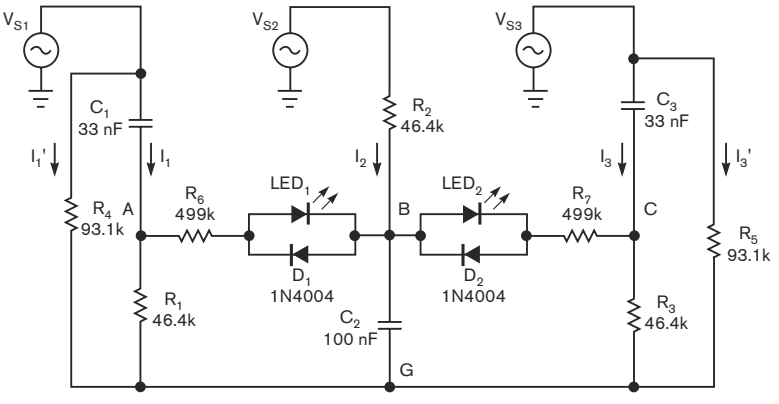

Figure 3 This phase-indicator circuit balances branch voltages and currents and requires no ground reference. These component values are for a 60-Hz line frequency.

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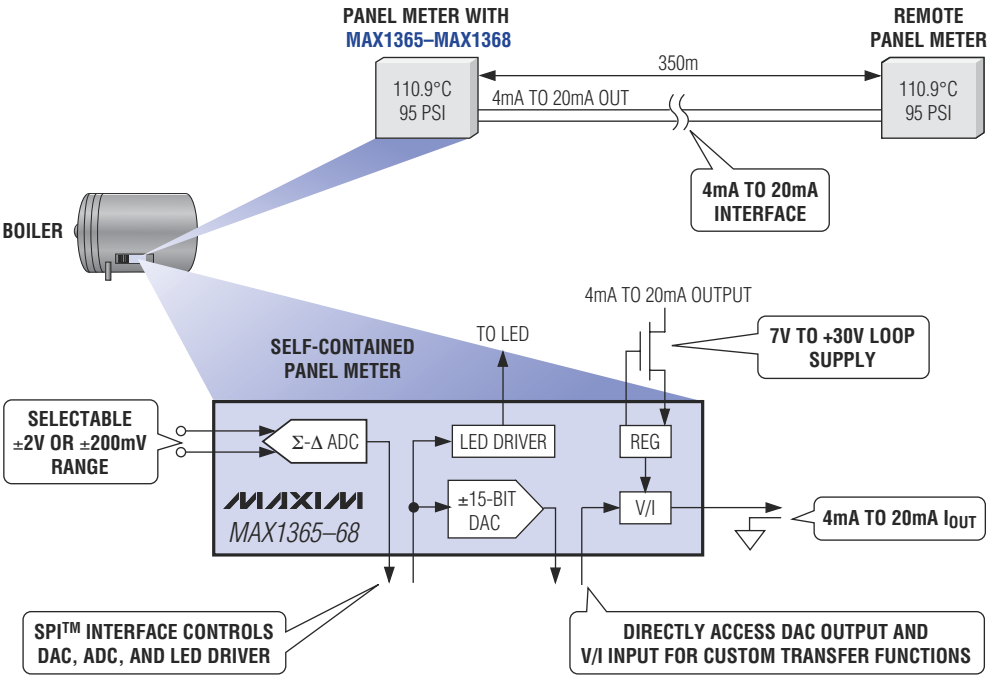

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Microcontroller's single I/O-port line drives a bar-graph display

R Jayapal, PhD, Bharat Heavy Electricals Ltd, Trichy, India

Instrument designs featuring a digital display may benefit from a secondary display that provides an analog version of the displayed parameter. A bar-graph display provides an easily interpreted graphical indicator that allows comparison with its full-scale value, but a conventional microcontroller-based design uses at least one eight-line I/O port to drive an eight-segment-bar-graph LED display.

As an alternative, some microcontrollers include a PWM (pulse-width-modulated) output. You can minimize the number of required I/O lines by using the PWM output to drive National Semiconductor's (www.national.com) LM3914 bar-graph-display-driver circuit or an equivalent. In operation, the microcontroller's program adjusts the PWM output's pulse width such that the average voltage that feeds to the LM3914 circuit illuminates the required number of bars in the display.

The design in **Figure 1** obviates the shortcomings of these approaches and uses only one port line to drive an eight-segment bar graph. This design does not use a PWM output and hence can apply to any microcontroller. Referring to the timing diagram in **Figure 2**, whenever the bar-graph display requires an update, the microcontroller's software delivers a pulse train through its output port. The first pulse comprises a pulse of width T_1 that's longer than the width of the pulse T_2, which triggering monostable IC_1, a 74123 or equivalent, produces. You apply both pulses to IC_3, a 7400 or equivalent NAND gate, which together with IC_1 forms a long-pulse detector. Use the equation in IC_1's data sheet to select values for C_1 and R_1 that yield a value of approximately 1.5 msec for T_2's output pulse. Typical widths for T_1 and T_3 are 3 and 1 msec, respectively.

The output pulse from IC_3 goes low for a duration of T_1-T_2, and this pulse clears IC_2, an 8-bit serial-in parallel-out shift register, which forces all of IC_2's outputs to go low and lights all segments of the bar-graph array (LED_1 to LED_8).

To light N segments of the bar-graph array, the microcontroller immediately sends a serial train of (8−N) pulses of width T_3 through the output-port line. Because the width of these pulses is less than T_2, NAND gate IC_3's output always remains high and thus does not clear the shift register. The rising edge of each of the microcontroller's output pulses loads a high to one of IC_2's outputs.

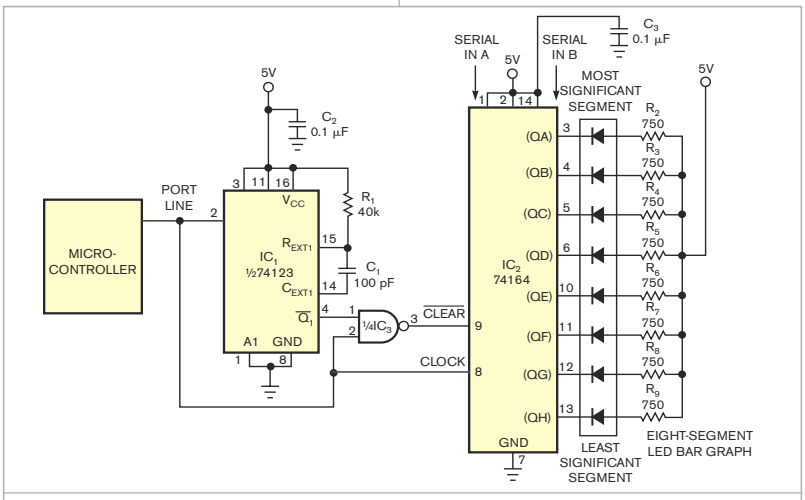


Figure 1 You can add a multisegment bar-graph display to a microcontroller that has only one output line.

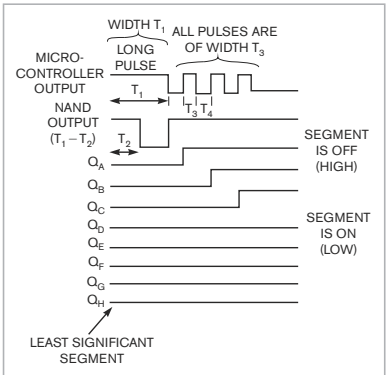


Figure 2 During the first pulse of the microcontroller's output-pulse sequence, the NAND gate's output clears the shift register and lights all of the display's segments.

Note that shift register IC_2's QA output connects to the bar graph's most significant segment. Hence, the first pulse switches off the most significant segment. Starting with the most significant segment, for (8−N) pulses, 8−N segments switch off, and N segments beginning with the least significant segment remain lighted. Using this reverse logic takes advantage of the shift register's outputs' ability to sink more current than they can source—8 versus 0.4 mA, respectively, and thus produce a brighter bar-graph display without adding output buffers. **Figure 2** shows a sample timing diagram that lights five of eight display segments.

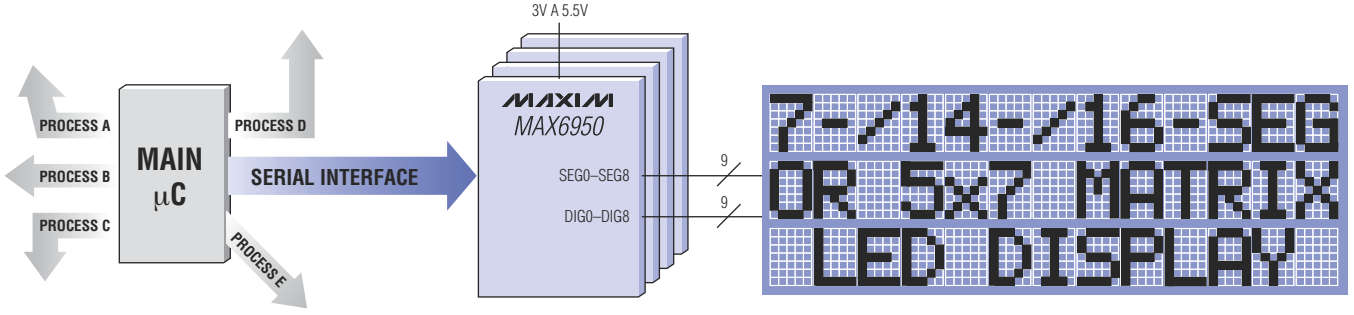
If a second output-port line is available, you can omit using monostable multivibrator IC_1 and NAND gate IC_3 and use the second port to clear the shift register by outputting a zero whenever the bar graph requires an update. To obtain finer resolution, you can add segments to the bar graph by cascading additional shift registers. To light N segments of a display that is M segments long, the first output port sends M−N pulses to the shift register's clock input.

This design lends itself well to situations in which unused I/O-port lines are at a premium, as is the case for microcontrollers with reduced pin counts, or if you need to retrofit a bar-graph display by adding a daughterboard to a design. EDN

3V TO 5V LED DISPLAY DRIVERS SIMPLIFY SOFTWARE AND SPEED DEVELOPMENT

Interface Directly to Main µP with Integrated Multiplex Engine, Digital Brightness Control, Blink, and Fonts

The MAX6950–MAX6959 are LED display drivers for 5 x 7 matrix and 7-, 14-, and 16-segment displays. These devices feature an integrated multiplex engine, fonts, keyscan, blink, and intensity control. Easily controlled through a serial interface by the main microprocessor (µP), these display drivers eliminate the need for a separate front-panel microcontroller (µC).



- Choice of Serial Interface
  - 400kHz I²C*-/SMBus™-Compatible
  - 26MHz SPI™-Compatible
- Power-Saving 3V Operation
- Embedded ASCII Fonts
- Integrated Keyscan (MAX6954/MAX6955/MAX6959)
- Available in Space-Saving Surface-Mount and DIP Packages

Part	Interface (Hz)	Supply (V)	Display Type	Total No. of LEDs	Fonts	Package
MAX6950	26M SPI	2.7 to 5.5	5 digits/7 segment + DP	40	Hex	16-QSOP
MAX6951	26M SPI	2.7 to 5.5	8 digits/7 segment + DP	64	Hex	16-QSOP
MAX6952/MAX6953	26M SPI/400k I²C	2.7 to 5.5	4 digits/5 x 7 matrix	140	104 fixed plus 24 user-definable characters	40-DIP/36-SSOP
MAX6954/MAX6955	26M SPI/400k I²C	2.7 to 5.5	16 digits/7 segment + DP 8 digits/14 or 16 segment + DP	128	104 fixed plus 24 user-definable characters	40-DIP/36-SSOP
MAX6956/MAX6957	400k I²C/26M SPI	2.7 to 5.5	Static (any type)	20 or 28	—	28-DIP/SSOP, 40-DIP/36-SSOP
MAX6958	400k I²C	3 to 5.5	4.5 digits/7 segment + DP	36	Hex	16-DIP/QSOP
MAX6959	400k I²C	3 to 5.5	4.5 digits/7 segment + DP	32	Hex	16-DIP/QSOP

*Purchase of I²C components of Maxim Integrated Products, Inc., or one of its sublicensed Associated Companies, conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.
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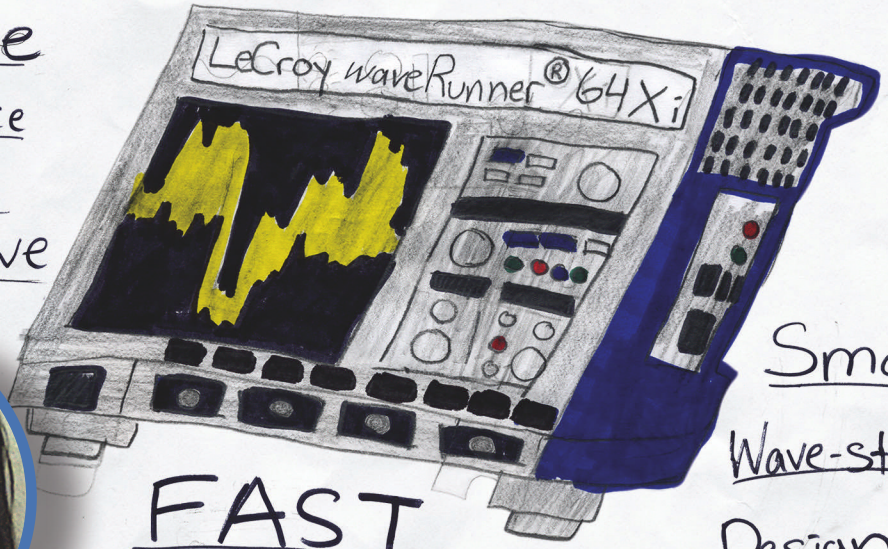
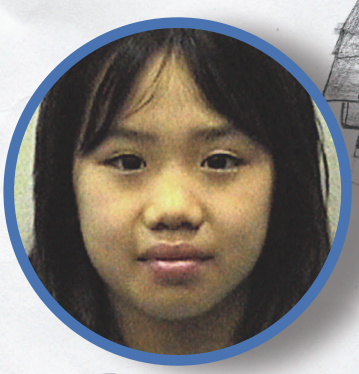
Effective



Small
Wave-stream
Design
Worldwide

FAST



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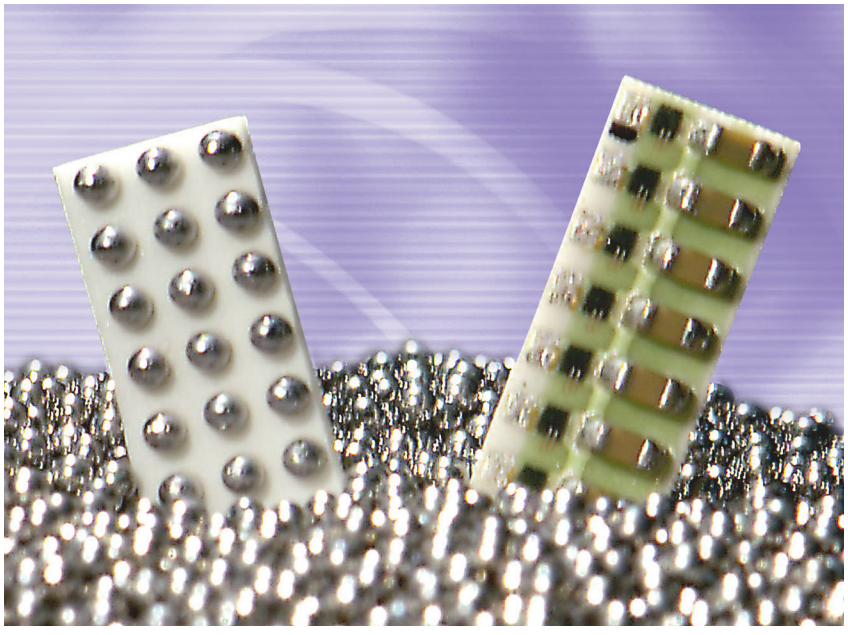
PASSIVES



Network performs high-speed data-line termination

Performing termination for high-speed memory buses, the BB1110RC resistor-capacitor network also includes decoupling functions for high-frequency data-line drivers. Features include nine 50Ω resistors in series with nine X5R 10V/0.1-µF capacitors in a center-bused schematic, a ±1% resistor tolerance, a ±10% capacitor tolerance, and a 200-ppm/°C TCR. Providing a 0.05W resistor-power rating and a 1W overall package power rating, the BB1110RC costs $1.

BI Technologies, www.bitechnologies.com

Electrically programmable resistors come in dual configuration

The Rejustors target analog-compensation problems in the analog domain. Available in an SOIC-8 configuration, these electrically programmable resistors are user-programmable to a fixed resistance with high precision and stability. You can adjust these devices hundreds of times, and they maintain the most recent adjustment state when in storage for extended periods. After trimming, these passive devices require no power to hold their value. Available in dual configurations including 4.7-, 10-, and 15-kV options, Rejustors cost 30 cents to $1.50, depending on packaging and volume. Trimming tools, including the MBK-408 and Matchbox, are available to develop familiarity with the Rejustor.

Microbridge Technologies, www.mbridgetech.com

Thick-film chip-resistor dividers come in versatile packaging

A small 2512 case and a choice of top-only or wraparound terminations make the CDHV thick-film chip-resistor dividers appropriate for high-voltage power supplies, power-switching equipment, and inverter controls. Features include less than 0.03% ratio stability at full power, a 3-kV handling voltage, and a 100-ppm/°C TCR. The CDHV costs $1.95.

Vishay Intertechnology, www.vishay.com

Ceramic multianode chip capacitors have low ESR

The CoreCAP NPV series of niobium-oxide ceramic multianode chip capacitors target power-management decoupling and dc/dc-converter filtering. The devices feature low ESR (equivalent series resistance), high ripple-current absorption, and high reliability. Aiming at telecom-networking, servers, embedded-computer systems, and notebook-computer markets, the series features less than 3-mΩ ESR rates and a 560-µF capacitance range with a ±20% capacitance tolerance. Supporting a −55 to +105°C temperature range, the CoreCap NPV series chip capacitors cost $1.28 (10,000).

AVX Corp, www.avx.com

DPP offers an alternative to DACs

Adding to the vendor's DPP (digitally-programmable-potentiometer) family, the 15V, 128-tap, 7-bit CAT-5133 targets calibration and control functions in high-voltage consumer, industrial, and medical applications. Functioning as an alternative to DACs and

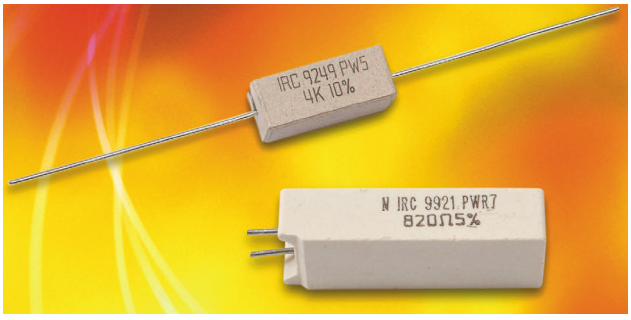
PASSIVES

mechanical potentiometers, this device requires no external memory or additional interconnects. Instead of a charge pump, the units have a separate input for an analog supply as high as 15V, providing the high-voltage bias for potentiometer terminals and eliminating charge-pump noise. An on-chip nonvolatile EEPROM retains settings if power is lost. You can preset the wiper position to any position on the device, and, on power-up, the wiper goes to the preset position stored in the EEPROM. The DPP uses an increment/decrement interface and costs 88 cents (1000).

Catalyst Semiconductor, www.catsemi.com

Power wirewound resistors have 60W power ratings

Capable of handling overload conditions, the high-powered, flameproof PW and PWR series power wirewound resistors come in high-temperature ceramic shells and with 60W power ratings. The devices target industrial, automotive, and



appliance applications. The PW series features 2 to 25W power ratings in axial-lead configurations and 20 to 60W in radial-terminal configurations; these devices are available in 0.10Ω to 30 kΩ resistance values, at ±5% or ±10% tolerances. TCRs are 300 to 5500 ppm/°C. PWR-series resistors are radial-leaded devices with 3 to 10W power ratings, 0.10Ω to 18 kΩ resistance values, and ±5% or ±10% tolerances. Devices in the PW series cost 15 to 20 cents (10,000), and PWR-series devices cost 43 cents (10,000).

IRC, www.irctt.com

INTEGRATED CIRCUITS

Radio-transmitter IC has high power efficiency

Claiming 30% lower battery-power consumption at the same transmission range as competing products, the MICRF405 radio-transmitter IC offers ASK/OOK (amplitude-shift-keying/on-off-keying) and FSK (frequency-shift-keying) modulation and covers the 315-, 433-, 868-, and 915-MHz bands. This device addresses the trend of migration from simple ASK/OOK-modulation devices to FSK devices featuring higher output power and longer range. Targeting high-end remote keyless entry, automatic meter reading, building automation, and industrial-control applications, the IC costs $1.48 (10,000).

Micrel, www.micrel.com

Analog switch handles negative signals

Handling negative signals with a single positive power supply allows the MAX4910 quad SPDT (single-pole-double-throw) analog switch to reduce external component count and improve audio-signal quality. This device depletes the capacitive charge that builds up on the unconnected port of the switch to ground, reducing audio click-and-pop sounds. Features include a 0.37Ω on-resistance, a 0.35Ω on-resistance

flatness, and a 0.05% total harmonic distortion. Operating from −40 to +85°C, the device comes in a 3×3-mm TQFN-16 package and costs $1.34 (1000).
Maxim Integrated Products, www.maxim-ic.com

Versatile RF synthesizers have a high output frequency

This STW8110X family of integrated single-chip RF synthesizers with embedded VCOs (voltage-controlled oscillators) has an available output frequency greater than 3 GHz. Targeting radio applications from cellular base stations to satellite communications and CATV equipment, the device has 0.2° rms at 1 GHz, 0.5° rms at 2 GHz, and 1.3° rms at 4-GHz measured values with a 200-kHz frequency step. The devices have automatic center-frequency calibration and a multiple-output option, allowing them to operate at multiple bands over a 750-MHz to 4.65-GHz spectrum. The product family also features a dual digital interface with I^2C protocol for connecting multiple devices, and an SPI bus. The STW81101 and STW81102 cost $3 each.
STMicroelectronics, www.st.com

Power amplifier targets enhanced-data-rate Bluetooth applications

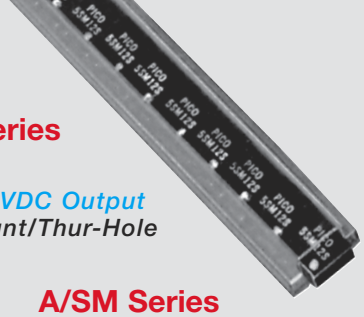
Using a miniature power amplifier, the SE2425U RangeCharger ICs target standard Bluetooth and EDR (enhanced-data-rate) applications. Based on a high-efficiency silicon-germanium architecture, the amplifier allows EDR support over longer distances for Bluetooth-capable cellular handsets, PDAs, wireless headsets, laptop computers, and cordless telephones. The Bluetooth SIG (Special Interest Group) developed the EDR protocol, which enables Bluetooth wireless connections with 3-Mbps bandwidth, boosting transmission ranges to 100m. This integrated power amplifier includes an input match, interstage matching, and CMOS-enable circuitry. Available in a 3×3×0.5-mm QFN-16 package, the SE2425U costs 95 cents (10,000).
SiGe Semiconductor, www.sige.com

Analog switches provide low on-resistance

Three dual SPDT (single-pole-double-throw) monolithic CMOS analog switches target use in portable and battery-powered products. Available in lead-free DFN-10 or MSOP-10 packages, the DG2731, DG2732, and DG2733 analog switches use a submicron-CMOS-low-voltage-process technology that provides 300-mA latch-up protection

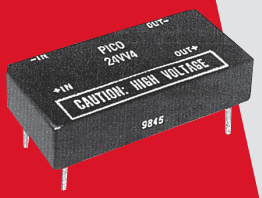
DC-DC Converters
2V to 10,000 VDC Output

New AV Series
Isolated
100 to 5000 VDC Output
Surface Mount/Thur-Hole

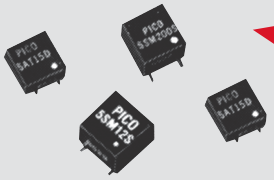


New Dual Isolated Outputs
to 250 VDC Isolated Output
Thru-Hole and Surface Mount

VV Series
Up to 10,000 VDC Output
Up to 10 Watts



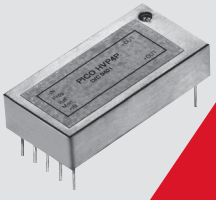
A/SM Series
Surface Mount/Thur-Hole
Isolated
3.3 to 1000 VDC Output



AVR Series
Regulated to IKV
Low Noise

M/MV Series
Military Components
Military Environmental
Testing Available
3.3 to 500 VDC

HVP Series
Programmable to
6000 VDC Output



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Isolated to
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LV/HV Series
36 to 170 Inputs
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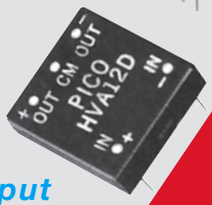
3.3 to 48 VDC Output



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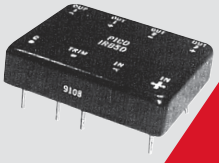
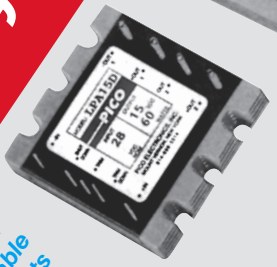
Wide Input Range
8 to 60 VDC
2 to 100 VDC Output
Regulated





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in 1/2 Brick and Full Brick

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Watts to 75 Watts
2 to 100 VDC Output Full Brick

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productroundup

INTEGRATED CIRCUITS

that complies with JESD78. Operating from single 1.6 to 4.3V supplies, the switches feature a 0.4Ω on-resistance at maximum power and a 0.03Ω delta on-resistance, lowering distortion and improving signal fidelity. A logic compatibility of 1.6V eases interfacing with low-voltage DSP or microcontroller logic. One-cell lithium-ion batteries directly power the switches, which, at 4.3V, have a 50-nsec turn-on time and a 14-nsec turn-off time. The DG2731 and DG2732 have two control pins with reverse-control logic; the DG2731 has two switches that are normally open and two that are normally closed, and the DG2732 has three normally open switches and one normally closed switch. The DG2733 has two normally open and two normally closed switches, as well as an "enable" pin for situations in which the logic is high. The switches cost $1.40 each (1000).

Vishay Intertechnology, www.vishay.com

EMBEDDED SYSTEMS

AdvancedTCA backplane uses dual-star and mesh configurations

This 14-slot AdvancedTCA full-mesh backplane features an 18-layer stripline design with a pluggable fan tray, a shelf manager, and power-entry connectors. Dual-star- or mesh-configuration options allow engineers to increase design flexibility. AdvancedTCA features include gigabit-per-second/terabit-per-second bandwidth across each shelf, 150 to 200W per board, and 3 kW per chassis power. Accommodating 8U×280-mm boards on a 1.2-mm pitch, the 14-slot AdvancedTCA backplane costs $2000.

Elma Bustronic Corp, www.bustronic.com

Rugged Flash disk card comes in XMC and PMC formats

Suiting applications in harsh environments that deal with extreme temperature, shock, or vibrations and making use of mechanical hard-disk drives impractical, the PBOD Flash-disk PMC or XMC card provides 64 Gbytes of high-

EMBEDDED SYSTEMS

speed storage. Features include as many as 10 Mbps; more than 40 Mbps of aggregate performance; software support for multiple RAID levels; and a PMC 32-bit, 33/66-MHz, or XMC one-lane PCI Express card. Offering L0, L50, and L100 air-cooled configurations, the device also comes in L100 and L200 conduction-cooled ruggedized levels. Also available in 16-, 24-, 32-, and 64-Gbyte configurations, an 8-Gbyte PBOD costs $2500.
Curtiss-Wright Controls Embedded Computing, www.cwcembedded.com

CPU features Dual-Core Intel Xeon processor

The Eurocom 400 CPU features the 2-GHz Dual-Core Intel Xeon LV processor with a COM Express platform. The device yields a higher system performance using the E7520 chip set and an eight-lane PCI Express connection to the carrier board. The modules allow simultaneous data transfer on gigabit Ethernet and simultaneous access to RAID, allowing the implementation of 4 Gbytes of RAM with ECC. Additional features include 31W power consumption and internal graphics. Available with a carrier board with complete I/O for development and standard production applications, the Eurocom 400 COM Express module costs $1499.
American Eltec, www.americaneltec.com

Evaluation platform supports the vendor's 8051 microcontroller

The VersaKit-20xx evaluation platform provides support for the VRS51L2070 Versa 8051 microcontroller. Allowing system prototyping and design development, the kit includes a development board, a VersaJTAG programming/debugging interface, a DB25 parallel cable, and a power supply. The VersaKit-20xx costs $99.
Ramtron Internation Corp, www.ramtron.com

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Summer 2006

Currents Quarterly

Your first look at new analog and mixed-signal ICs

Power Management

New CPU power controller enables greater system stability and reliability for computing and gaming platforms

The ADP3192 is an advanced power controller IC for notebook, desktop, and gaming platform applications. The ADP3192 combines ADI's proprietary enhanced pulse-width modulation (EPWM) and Flex-Mode™ architectures that provide faster response time and regulation of power supplies while at the same time dramatically reducing the number of on-board capacitors by up to 50%, giving designers the tools needed to reduce overall board space by as much as 30%, and lowering motherboard costs by as much as 15%. The ADP3192 is specifically designed to predict and adjust to accommodate system power transients, thus ensuring a more stable operating environment. The ADP3192 comes in a 6 mm × 6 mm, 40-lead LFCSP package.

ADP3192 $1.30

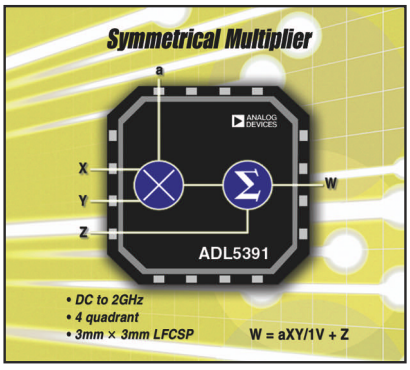
World's smallest I²C® inductor flash LED driver dramatically extends battery life in portable electronic devices

The ADP1652 is a new I²C-enabled IC solution designed for high efficiency flash solutions in handsets. The solution provides up to 52 lumens of brightness in flash mode, and achieves 92% of boost efficiency in video mode. With only four external components, this solution fits in an ultracompact 6 mm × 6 mm footprint. The ADP1652 dramatically extends battery life for new generations of low profile camera-enabled handsets, without sacrificing space budget. The ADP1652's integrated I²C interface enables full digital programmability of the drivers' current and the flash timer. The ADP1652 comes in a compact, 3 mm × 3 mm, 16-lead LFCSP package.

ADP1652 $1.95

For FREE samples, data sheets, and more information on these products, go to *www.analog.com/currentsquarterly*.

RF and Communications



DC to 2 GHz analog multiplier delivers gain and modulation control within wideband communications applications

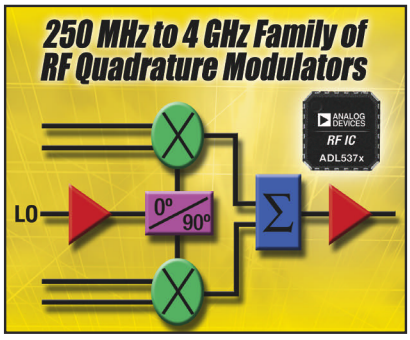
In wideband communications applications such as adaptive antenna systems and power amplifier correction circuits, the task of multiplying high frequency analog signals for gain and modulation control can now be realized by Analog Devices' latest dc to 2 GHz analog multiplier. Drawing on three decades of experience in advanced analog multiplier products, the new ADL5391 allows fully symmetrical linear control of the IC's three inputs interfaces: X, Y, and Z. If you are seeking versatility in function synthesis via the math function, W = aXY/1V + Z, then visit our website to learn more about the ADL5391, view the data sheet, and order samples. And don't forget that ADI also has a broad range of mixers, modulators, multipliers, demodulators, detectors, frequency synthesizers, and VGAs, as well as converters and other RF/IF products.

ADL5391	$4.98

Power accurate RF measurement and control in a small package

The ADL5500 offers unrivaled temperature stability and accuracy while measuring the rms/TruPwr™ level of complex waveforms used in 3G+ communication systems. The small size and high level of integration are additional features that make the ADL5500 ideal for cellular handsets where size and power consumption are very critical. Not all customers are comfortable handling and manufacturing their end products with such a small device. To meet their requirements, ADI has developed the ADL5501, which implements these performance features of the ADL5500 in a small, 6-lead SC70 package with a footprint of less than 2 mm × 2 mm. The ADL5501 offers increased flexibility by including one pin for an optional external filter capacitor and another for an enable pin.

ADL5500	$0.90
ADL5501	$0.90



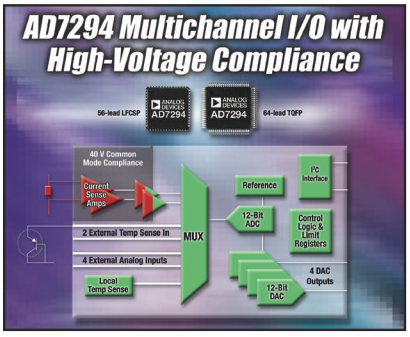
New family of pin-compatible modulators delivers best performance and value from 250 MHz to 4000 MHz

Selecting a single broadband direct conversion modulator to handle the multitude of frequency bands used in wireless and broadband communications networks results in many trade-offs and performance degradation at the extreme ends of the device operating frequency. These performance trade-offs are further compromised by part-to-part and temperature variations. ADI's new family of FMOD ADL537x series of modulators are pin-compatible, sharing the same 24-lead, 4 mm × 4 mm LFCSP package, and cover a frequency range of 50 MHz to 4 GHz. The FMOD family provides the highest output power and linearity, alleviating the problem associated with devices that degrade in performance at the extreme end of their frequency bands. Each family member is optimized for a specific band of operation, offering outstanding dynamic range at the highest possible output power. The new FMOD family is the ideal choice for direct conversion applications supporting 2G, CDMA, GSM, new 3G-CDMA radios, and future 4G, WiMAX, and 3.8 GHz radios.

ADL5370	$4.98
ADL5371	$4.98
ADL5372	$4.98
ADL5373	$4.98
ADL5374	$4.98

For FREE samples, data sheets, and more information on these products, go to *www.analog.com/currentsquarterly*.

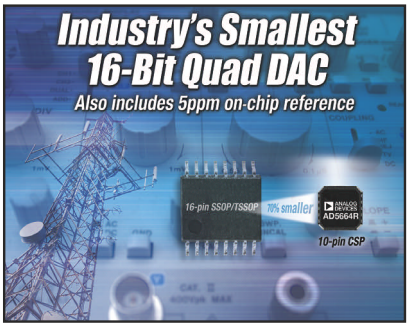
Data Converters



Multichannel I/O data converter with high voltage compliance for wireless base station

The AD7294 multichannel input/output (I/O) data converter integrates, in a single chip, all the functions required for the monitoring and control of current, voltage, and temperature in wireless base stations. It integrates a 4-channel, 12-bit DAC, a 9-channel, 12-bit ADC, two high-side current sense amplifiers, and three temperature sensor channels (one internal, two external). This solution improves performance and reliability, and significantly reduces component count and cost, when compared with traditional solutions that consisted of many discrete components. The AD7294 is an easy to use, compact solution for wireless base station designers. Comes in an 8 mm × 8 mm, 56-lead LFCSP package and a 64-lead TQFP.

AD7294 $9.00



The industry's smallest, most integrated 16-bit quad DAC

The AD5664R is the industry's first 16-bit quad DAC in a compact, 3 mm × 3 mm, 10-lead LFCSP. It offers 16-bit resolution at a 70% reduction in board space over existing solutions. Not only is this the smallest DAC in its category, it also integrates an on-chip 5 ppm/°C reference. Consuming only 5 mW at 5 V, the combination of performance, integration, and small footprint is ideal for designers of PLC cards, analog I/O boards, and many other space-constrained systems. The AD5664R is part of a family of devices providing 12-bit to 16-bit pin-compatible solutions for process control, data acquisition systems, portable battery-powered instruments, and digital gain and offset adjustment.

AD5664R $10.45

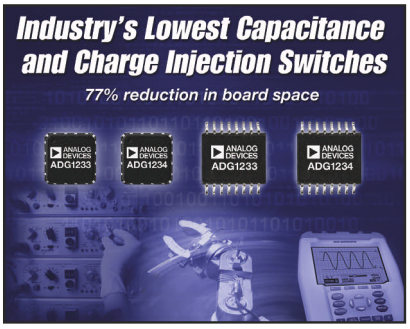
18-bit, single-channel DAC is newest member of *nano*DAC® family

The AD5680 is a single-channel, buffered voltage-output DAC that combines 18-bit resolution and 12-bit accuracy, in a space-efficient, 8-lead SOT-23. It is ideal for low bandwidth (1 kHz range), space-constrained, closed-loop, process control applications that require precision control. It has an on-chip output amplifier, operates within an extended industrial temperature range of –40°C to +105°C, and dissipates just 750 μW at 5 V.

AD5680 $3.39

For FREE samples, data sheets, and more information on these products, go to *www.analog.com/currentsquarterly*.

Switches

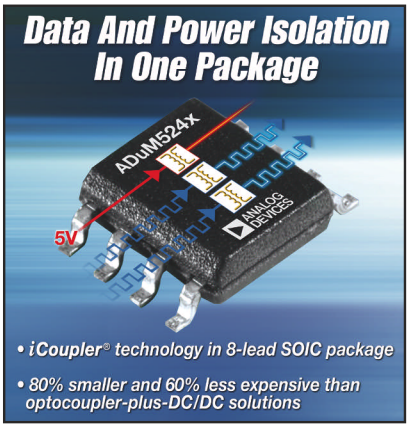


Switches offer industry's lowest capacitance and charge injection for high end data acquisition applications

The ADG1233 and ADG1234 are triple and quad SPDT ±15 V/±12 V *i*CMOS™ switches, and deliver the industry's lowest capacitance and charge injection. These devices meet a need among industrial design engineers for analog switches that increase data acquisition speeds. Their low off capacitance (1.5 pF) and charge injection (<1 pC) make them ideal for high end data acquisition and sample-and-hold applications that require low glitch and fast settling times. The ADG1233 triple SPDT is provided in 16-lead TSSOP and 4 mm × 4 mm LFCSP packages, and the ADG1234 quad SPDT is offered in 20-lead TSSOP and 4 mm × 4 mm LFCSP packages.

ADG1233	$3.95
ADG1234	$3.95

Digital Isolators

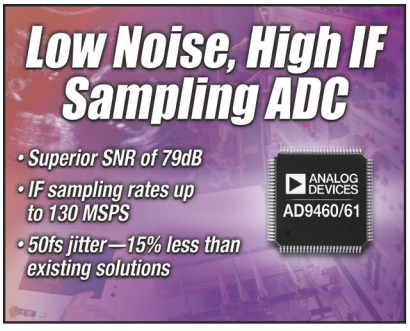


Dual-channel digital isolators with integrated dc-to-dc converter provide data and power isolation in one package

ADI's industry-leading family of *i*Coupler® digital isolators is extended with the introduction of the ADuM524x products that integrate a 50 mW isolated power supply with two digital signal isolators in an 8-lead SOIC package. The products incorporate ADI's new proprietary *iso*Power™ technology, using chip scale transformers to convey data and power across an isolation barrier. This eliminates the need for complex, sizeable, and costly combinations of optocouplers, transformers, and other components, thereby reducing cost by as much as 70% and board space by as much as 80%. All come in narrow-body SOIC 8-lead packages.

ADuM524x	$2.95

A/D Converters

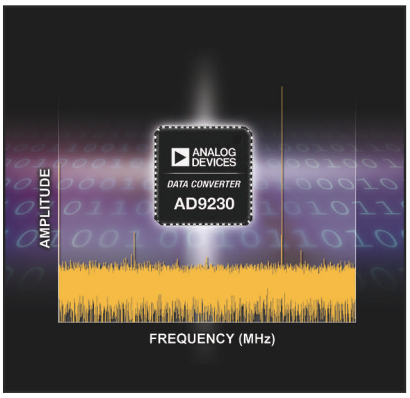


New wideband ADCs deliver true 16-bit resolution for instrumentation, radar, medical imaging, and communication systems

The AD9460 and AD9461 provide 16-bit performance at up to 130 MSPS, enabling the high dynamic range required for signal analysis, radar, magnetic resonance imaging (MRI), and multicarrier/multi-std wireless communications systems. In these designs, higher ADC sampling rates allow engineers to capture and digitize wider signal bandwidths and to handle higher Tesla magnetic fields for superior imaging in MRI. In addition, the AD9460 and AD9461 operate with lower power to aid in multichannel systems. The AD9460, offered at 80 MSPS and 105 MSPS sampling rates, consumes 1.4 W and 1.6 W, respectively. At its highest sampling rate of 130 MSPS, the AD9461 consumes 1.9 W. Both devices are packaged in a Pb-free, 100-lead TQFP/EP surface-mount package.

AD9460-80	$48.33
AD9450-105	$56.67
AD9461-130	$65.00

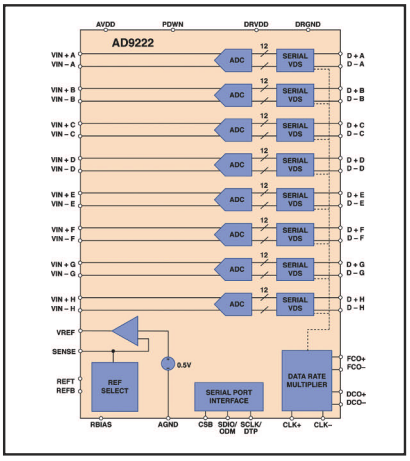
For FREE samples, data sheets, and more information on these products, go to *www.analog.com/currentsquarterly*.



New 12-bit, 250 MSPS, high performance A/D converter brings power consumption below the 500 mW barrier

The 12-bit, 250 MSPS AD9230 is the flagship device in a family of pin-compatible, low power, single-supply 1.8 V converters. The AD9230 dissipates only 425 mW of power at full sampling rate and is capable of maintaining excellent SNR (65.5 dBFS) and SFDR (82 dBc) with a 70 MHz input. The device, when used in the transmit path of picocell or microcell base stations to optimize power amplifier linearization, also facilitates more rapid system deployment by enabling smaller-sized end systems. In cable termination systems, growing demand for digital cable services is placing greater emphasis on bandwidth, calling for low power ADCs that allow higher channel density. The AD9230 is offered in three speed grades (250 MSPS, 210 MSPS, and 170 MSPS), and the fully pin-compatible 10-bit version, the AD9211, is also offered in three speed grades (250 MSPS, 200 MSPS, and 170 MSPS).

AD9230-170	$35.00
AD9230-210	$42.00
AD9230-250	$59.00
AD9211-170	$25.00
AD9211-200	$32.00
AD9211-250	$39.00

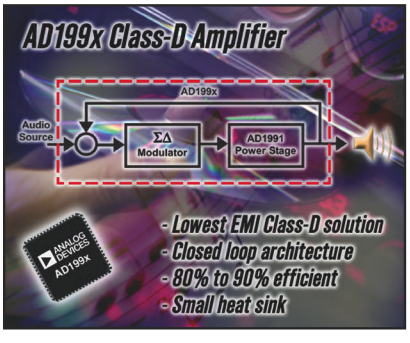


Low power, 8-channel, 12-bit and 10-bit ADC family provides LVDS interface, excellent dynamic performance at 65 MSPS, and small package size for high density applications

The AD9222 and AD9212 devices (12-bit/10-bit, respectively) provide eight channels of A/D conversion and dissipate only 119 mW per channel while operating at the full 65 MSPS. These devices represent a 30% smaller footprint and 4% to 5% less power than competing devices on the market. The ADCs contain several features designed to maximize flexibility and minimize system cost, such as programmable clock and data alignment and programmable digital test pattern generation. The available digital test patterns include built-in deterministic and pseudorandom patterns, along with custom user-defined test patterns entered via the serial port interface (SPI). The AD9222 and AD9212 are available in a Pb-free, 64-lead LFCSP package and are specified over the industrial temperature range of –40°C to +85°C.

AD9212-40	$32.00
AD9212-65	$40.00
AD9222-40	$44.00
AD9222-65	$65.00

Amplifiers



Class-D stereo audio amplifiers for advanced TV and automotive applications

The AD1994 Class-D amplifier integrates a stereo Σ-Δ modulator and stereo "bridge-tied" load (BTL) power stage onto a single die capable of delivering 50 W of continuous power without a heat sink. The new Σ-Δ modulator architecture uses a patented dynamic hysteresis algorithm to achieve audiophile performance (THD < 0.005%, SNR > 105 dB) without compromising efficiency. The closed-loop architecture and continuous-time modulator front end achieve a PSRR > 65 dB, and the stereo BTL power stage requires only a single supply that can operate over a wide voltage range. The Σ-Δ modulator in the AD1994, designed to minimize radiated and conducted EMI and RF emissions, can optionally be used to drive external power devices to achieve arbitrarily high output power. The device is packaged in a 64-lead LFCSP and operates over the –40°C to +85°C temperature range.

AD1994	$4.42

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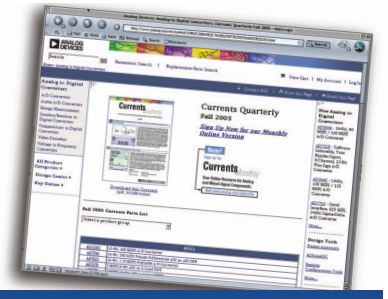
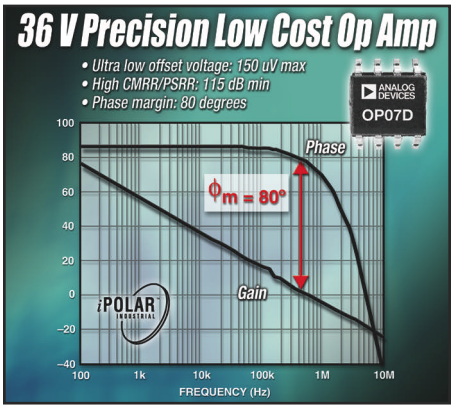


For a complete list of products released this quarter and to order samples, please visit *www.analog.com/currentsquarterly.*

Ultralow power, Sixth order video filter with power-down

The ADA4430-1 is a fully integrated video reconstruction filter that combines excellent video specifications with low power consumption and an ultralow power disable, making it ideal for portable video applications. With 0.5 dB frequency flatness out to 7 MHz and 50 dB rejection at 27 MHz, the ADA4430-1 is ideal in SD video applications, including NTSC and PAL. The ADA4430-1 operates on single supplies as low as 2.65 V and as high as 6 V while providing the dynamic range required by the most demanding video systems. The ADA4430-1 is available in a 6-lead SC70 package and is rated to work in the extended automotive temperature range of –40°C to +125°C.

ADA4430-1 $0.49



High precision, ultralow offset op amp

The OP07D is a low cost option of the OP07 family with voltage offset performance of 150 μV max. The OP07D is a precision, ultralow offset amplifier that integrates low power (1.1 mA typical), low input bias current (±1 nA maximum), and high CMRR/PSRR (130 dB). Operation is fully specified from ±5 V to ±15 V supply. The OP07D provides higher accuracy than industry-standard OP07-type amplifiers due to the Analog Devices *i*Polar™ process, which supports enhanced performance in a smaller footprint. The OP07D is fully specified over the extended industrial temperature range of –40°C to +125°C. The OP07D amplifier is available in 8-lead DIP and the popular 8-lead, narrow SOIC lead-free packages.

OP07D $0.44

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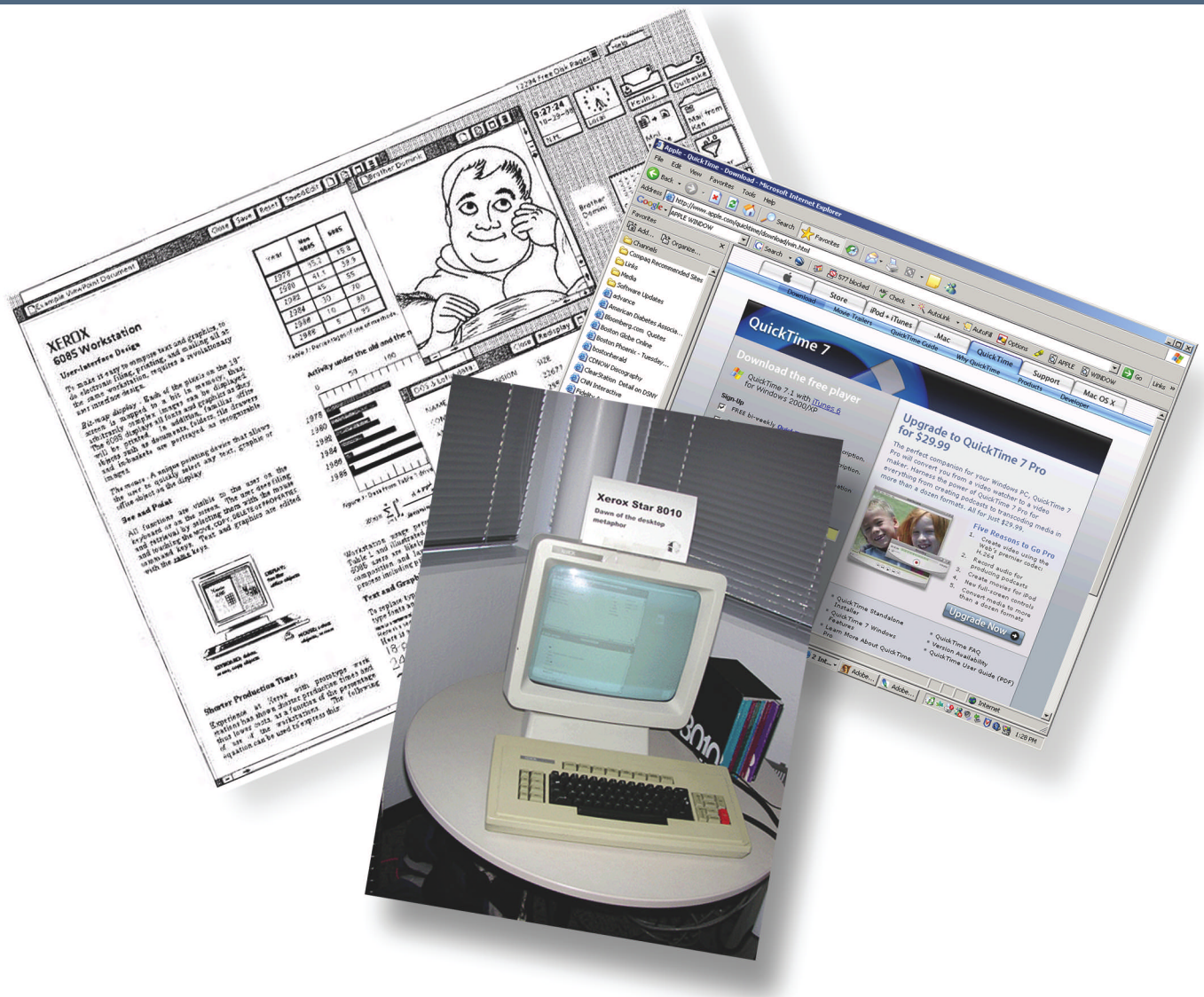

STATS First workstation with integral hard drive, more than 1 Mbyte of memory, GUI, and mouse

Xerox Star: The pioneer always gets the arrows

Few mistakes in the technological world are as deadly as the decision to lead the way with a brilliant product. That lesson is the big take-away from Xerox Corp's milestone, the 8010 workstation, better known by the code name of its software, Star. Gathering up innovations from Xerox PARC (Palo Alto Research Center) that ranged from microprogrammable CPUs to Smalltalk to the Ethernet to the mouse, Xerox took a technological leap and created a workstation that included them all—not just as a collection of hardware, but as components in a whole new way for humans to work with computers.

The result was a market catastrophe—too early, too expensive, and too slow to break through IT managers' perceptions of reality. But the 8010 became the cache of genius without which Sun, the Apple Lisa, the Macintosh, and Windows could not have existed. In this case, imitation wasn't sincere flattery; it was a grudging epitaph.—by Ron Wilson

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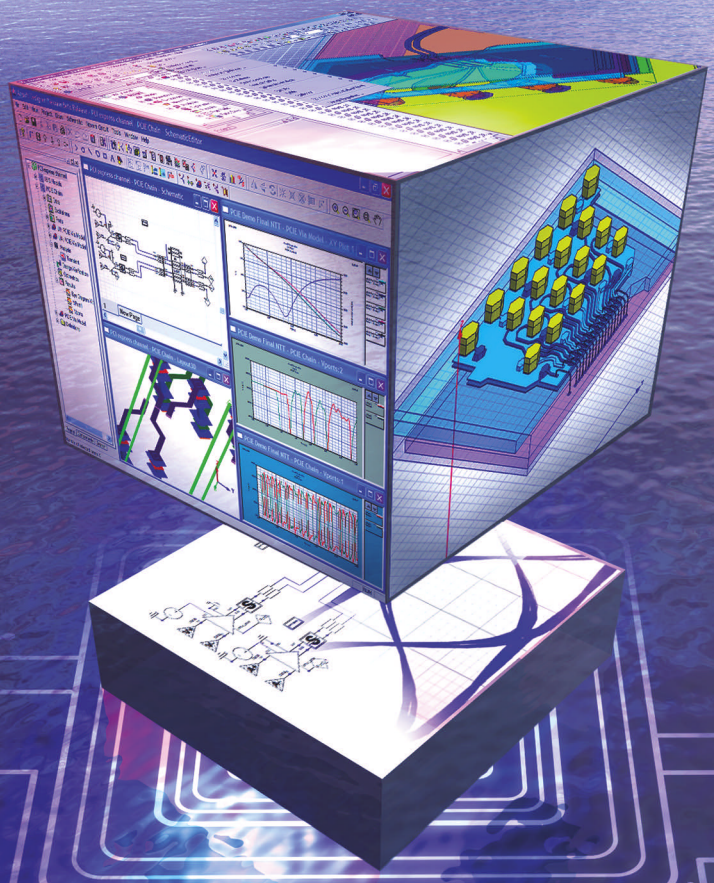

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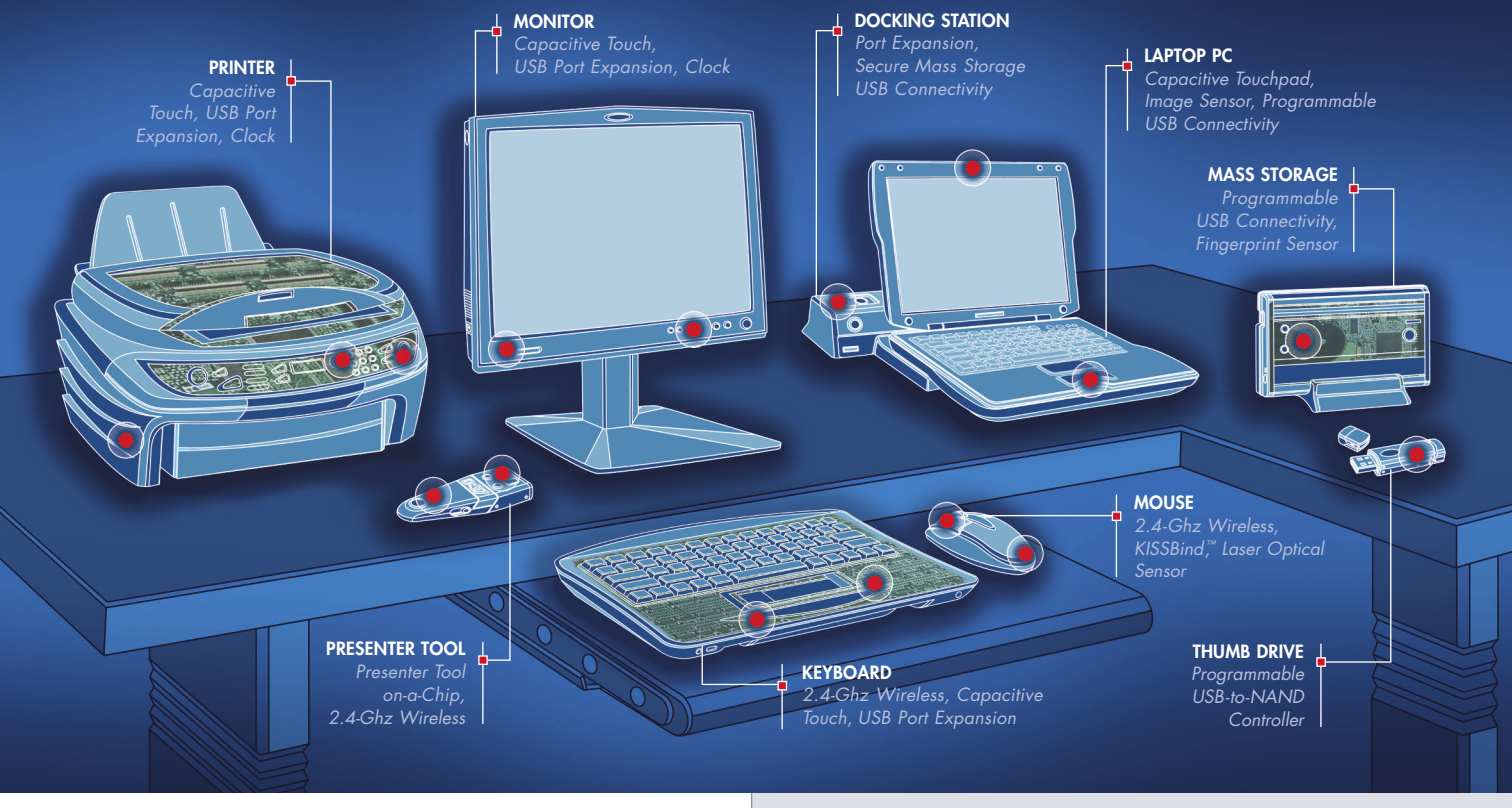

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